High-Performance DrBLADE

5 mm x 5 mm x 0.6 mm IQFN

TDA21310

Data Sheet

Revision 2.1, 2013-09-05

Power Management and Multi Market

Edition 2013-09-05

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Revision History	
Page or Item	**Subjects (major changes since previous revision)**
Revision 2.1 2013-09-05	
	Temperature Rise diagram added

1 Applications

- Desktop and Server buck-converter
- Single Phase and Multiphase POL
- CPU/GPU Regulation in Desktop Graphics Cards, DDR Memory, Graphic Memory
- High Power Density Voltage Regulator Modules (VRM).

2 Features

- Compatible to Intel® VR12 Driver and Mosfets Module (DrMOS) functionality for Desktop/Server Applications
- For synchronous buck converter step down voltage applications
- Power MOSFETs rated 25 V for safe operation under all conditions
- Fast switching technology for improved performance at high switching frequencies (> 1 MHz)
- +5 V high side and low side MOSFETs driving voltage
- Compatible to standard +3.3 V PWM controller integrated circuits
- Small package: LG-UIQFN-32-2 (5 x 5 x 0.6 mm³)
- Optimized footprint for improved cooling by the PCB
- DC output current up to 40A
- 94% peak efficiency at 1.2V[1]
- DC input voltage up to +16 V
- Remote driver disable function
- Includes bootstrap diode
- Undervoltage lockout
- Shoot through protection
- Tri-state PWM input functionality
- Top side cooling
- RoHS compliant

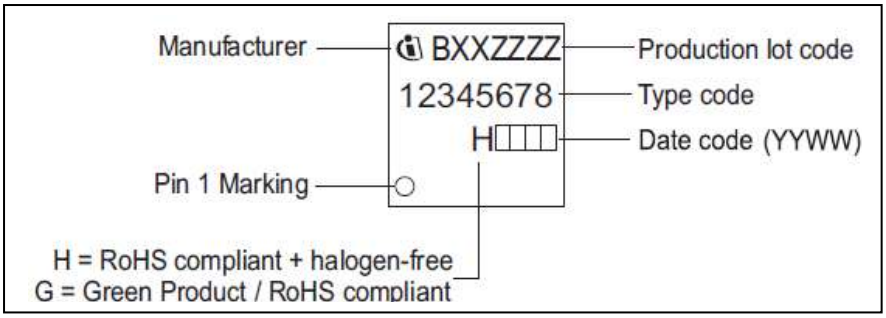


Table 1 Product Identification

Part Number	Temp Range	Package	Marking
TDA21310	-25 °C to 125 °C	LG-UIQFN-32-2 (5 x 5 x 0.6 mm³)	TDA21310

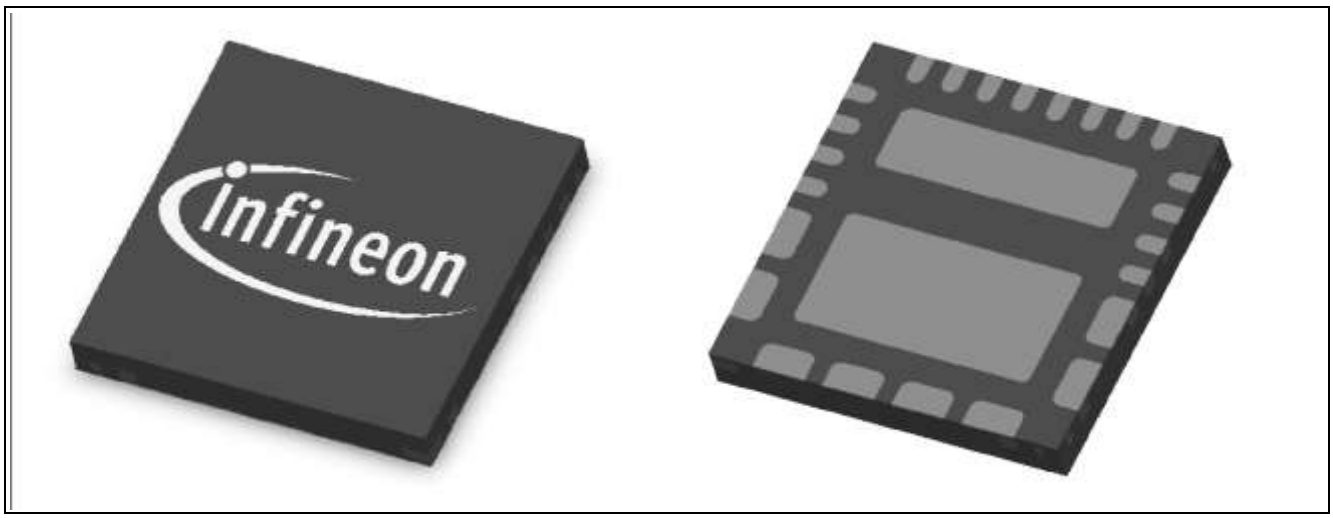


Figure 1 Picture of the Product

[1] Typical power stage efficiency, V_{IN}=12V, V_{DRV}=V_{CIN}=5V, f_{SW}=300kHz, L=210nH, 0.2mΩ, no air flow, no heat sink.

3 Description

3.1 Pinout

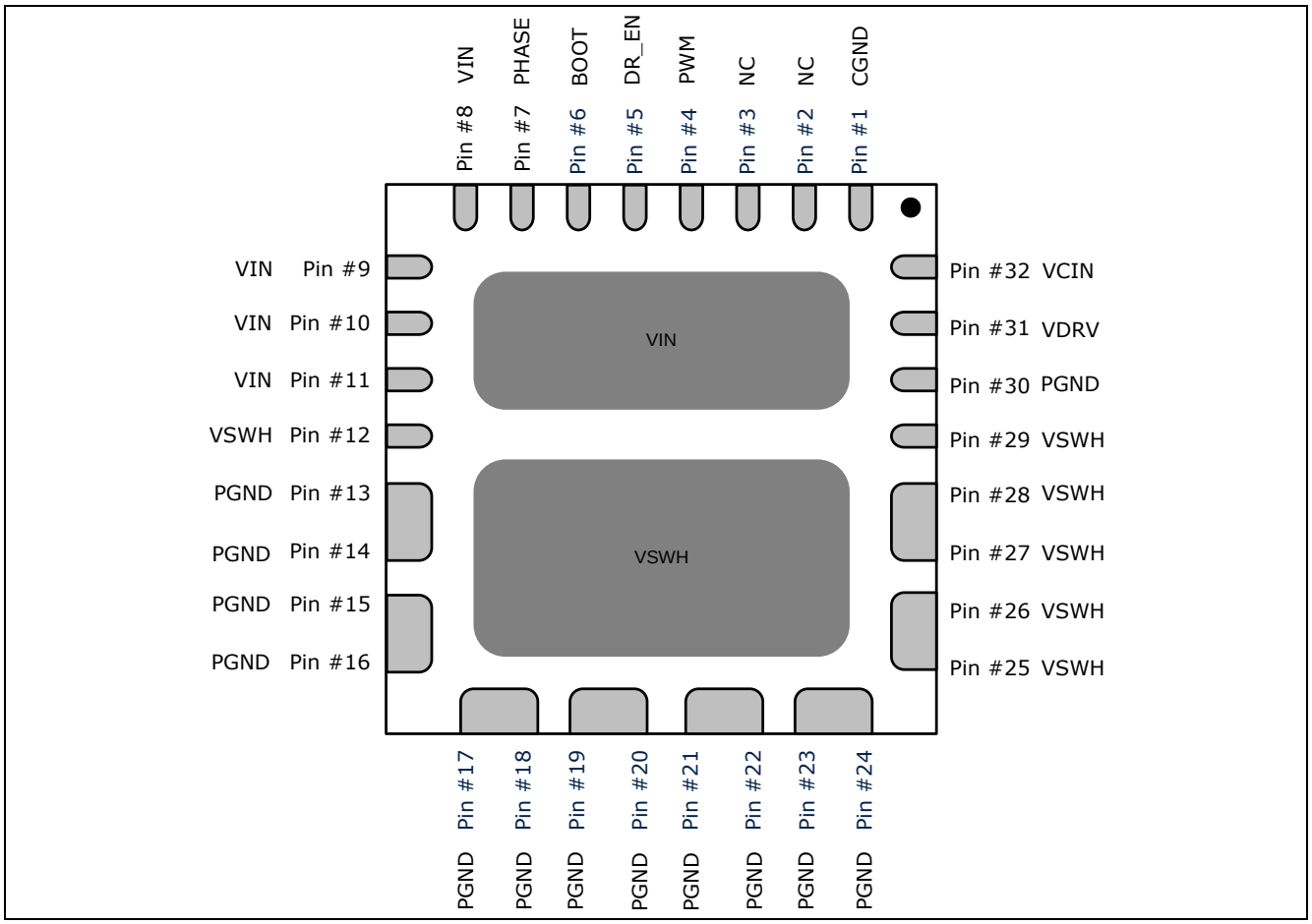


Figure 2 Pinout, numbering and name of pins (transparent top view)

Table 2 I/O Signals

Pin No.	Name	Pin Type	Buffer Type	Function
4	PWM	I	+3.3 V logic	**PWM drive logic input** The tri-state PWM input is compatible with 3.3 V.
5	DR_EN	I	+3.3 V logic	**Enable signal (active high)** Connect to GND to disable the IC.
6	BOOT	I	Analog	**Bootstrap voltage pin** Connect to BOOT capacitor
7	PHASE	I	Analog	**Switch node** (reference for Boot voltage) internally connected to VSWH pin, connect to BOOT capacitor
12, 25 to 29, VSWH pad	VSWH	O	Analog	**Switch node output** High current output switching node

Table 3 Power Supply

Pin No.	Name	Pin Type	Buffer Type	Function
8 to 11, VIN pad	VIN	POWER	–	**Input voltage** Supply of the drain of the high side MOSFET
31	VDRV	POWER	–	**FET gate supply voltage** High and low side MOSFETs gate drive supply
32	VCIN	POWER	–	**Logic supply voltage** 5 V bias voltage for the internal logic

Table 4 Ground Pins

Pin No.	Name	Pin Type	Buffer Type	Function
1	CGND	GND	–	**Control signal ground** Should be connected to PGND externally
13 to 24, 30	PGND	GND	–	**Power ground** All these pins must be connected to the power GND plane through multiple low inductance vias.

Table 5 Not Connected

Pin No.	Name	Pin Type	Buffer Type	Function
2, 3	NC	–	–	**No internal connection** Leave pin floating or tie to GND.

3.2 General Description

The Infineon TDA21310 is a multichip module that incorporates Infineon's premier MOSFET technology for a single high side and a single low side MOSFET coupled with a robust, high performance, high switching frequency gate driver in a single 32 pin LG-UIQFN-32-2 package. The optimized gate timing allows for significant light load efficiency improvements over discrete solutions. State of the art MOSFET technology provides exceptional full load performance.

When combined with Infineon's family of digital multi-phase controllers, the TDA21310 forms a complete core-voltage regulator solution for advanced micro and graphics processors as well as point-of-load applications.

The TDA21310 is not pin compatible to the Intel 6x6 DrMOS specification, but compatible by functionality. The device package height is only 0.6 mm, and is an excellent choice for applications with critical height limitations. It has reduced thermal impedance from junction to top case compared to DrMOS, allowing for top side cooling.

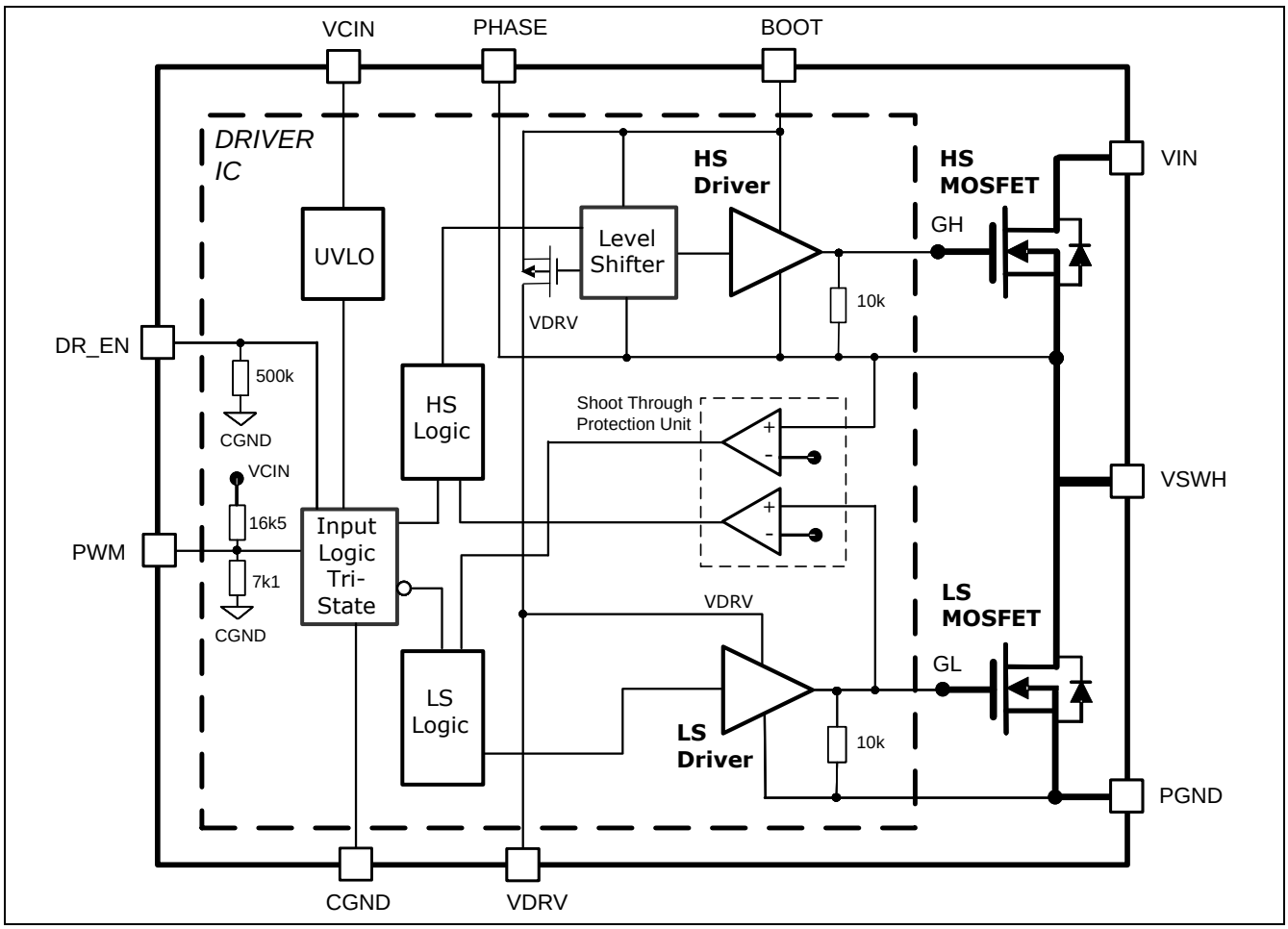


Figure 3 Simplified Block Diagram

Attention: GH and GL are not accessible. They are mentioned for clarity in this block diagram.

4 Electrical Specification

4.1 Absolute Maximum Ratings

Note: T_A = 25°C

Stresses above those listed in Table 6 “Absolute Maximum Ratings” may cause permanent damage to the device. These are absolute stress ratings only and operation of the device is not implied or recommended at these or any other conditions in excess of those given in the operational sections of this specification. Exposure over values of the recommended ratings (Table 8) for extended periods may adversely affect the operation and reliability of the device.

Table 6 Absolute Maximum Ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Frequency of the PWM input	f_{SW}	–	–	1.2	MHz	–
Maximum DC load current	I_{OUT}	–	–	40	A	–
Input Voltage	V_{IN} (DC)	-0.30	–	16	V	
Logic supply voltage	V_{CIN} (DC)	-0.30	–	6.5		–
High and Low side driver voltage	V_{DRV} (DC)	-0.30	–	6.5		–
Switch node voltage	V_{SWH} (DC)	-1	–	16		–
	V_{SWH} (AC)	-10[2]	–	25		–
PHASE node voltage	V_{PHASE} (DC)	-1	–	16		–
	V_{PHASE} (AC)	-10	–	25		–
BOOT voltage	V_{BOOT} (DC)	-0.3	–	22.5		–
	V_{BOOT} (AC)	-1[2]	–	31.5		–
	$V_{BOOT-PHASE}$ (DC)	-1	–	6.5		–
DR_EN voltage	V_{DR_EN}	-0.3	–	5.5		–
PWM voltage	V_{PWM}	-0.3	–	5.5		–
Junction temperature	T_{Jmax}	-40	–	150	°C	–
Storage temperature	T_{STG}	-55	–	150		–

Note: All rated voltages are relative to voltages on the CGND and PGND pins unless otherwise specified.

[2] AC is limited to 10 ns

4.2 Thermal Characteristics

Table 7 Thermal Characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance between driver junction and soldering point[3]	$\theta_{JS\text{-}driver}$	–	29	–	K/W	–
Thermal resistance between driver junction and top of package	$\theta_{Jtop\text{-}driver}$	–	14	–		–
Thermal resistance between high-side MOSFET junction and soldering point[3]	$\theta_{JS\text{-}HS}$	–	2	–		–
Thermal resistance between high-side MOSFET junction and top of package	$\theta_{Jtop\text{-}HS}$	–	7	–		–
Thermal resistance between low-side MOSFET junction and soldering point[3]	$\theta_{JS\text{-}LS}$	–	1	–		–
Thermal resistance between low-side MOSFET junction and top of package	$\theta_{Jtop\text{-}LS}$	–	2	–		–
Thermal resistance between driver junction and high-side MOSFET junction	$\theta_{JJ\text{-}driver\text{-}HS}$	–	40	–		
Thermal resistance between driver junction and low-side MOSFET junction	$\theta_{JJ\text{-}driver\text{-}LS}$	–	60	–		
Thermal resistance between low-side MOSFET junction and high-side MOSFET junction	$\theta_{JJ\text{-}LS\text{-}HS}$	–	36	–		

4.3 Recommended Operating Conditions and Electrical Characteristics

Note: V_{DRV} = V_{CIN} = 5 V, T_A = 25°C

Table 8 Recommended Operating Conditions

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input voltage	V_{IN}	5	–	16	V	–
MOSFET driver voltage	V_{DRV}	4.5	5	6		–
Logic supply voltage	V_{CIN}	4.5	5	6		V_{CIN} rising,3.3V to 3.9V: dv_{CIN}/dt > 300V/s
Junction temperature	T_{jOP}	-25	–	125	°C	–

[3] The junction-soldering point is referred to the bottom exposed pad.

Table 9 Voltage Supply And Biasing Current

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
UVLO rising	V_{UVLO_R}	–	3.5	–	V	V_{CIN} rising,3.3V to 3.9V: dv_{CIN}/dt > 300V/s
UVLO falling	V_{UVLO_F}	–	3.1	–		VCIN falling
Driver current	I_{VDRV_300kHz}	–	12	–	mA	DR_EN = 3.3V, f_{SW} = 300 kHz
	I_{VDRV_1MHz}	–	38	–		DR_EN = 3.3V, f_{SW} = 1 MHz
	I_{VDRV_PWML}	–	25	–	µA	DR_EN = 3.3V, PWM = 0 V
	I_{VDRV_PWMH}	–	12	–		DR_EN = 0V, PWM = 3.3V
IC current (control)	I_{VCIN_PWML}	–	400	–		DR_EN = 3.3 V, PWM = 0 V
	I_{VCIN_O}	–	500	–		DR_EN = 3.3 V, PWM = Open
IC quiescent	$I_{CIN}+I_{DRV}$	–	–	550		DR_EN = 0 V

Table 10 Logic Inputs And Threshold

Parameter		Symbol	Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
DR_EN	Input low	$V_{DR\_EN\_L}$	0.7	1.1	1.3	V	V_{DR_EN} falling
	Input high	$V_{DR\_EN\_H}$	1.9	2.1	2.4		V_{DR_EN} rising
	Sink current	I_{DR_EN}	–	2	–	µA	V_{DR_EN} = 1 V
PWM	Input low	V_{PWM_L}	–	–	0.7	V	V_{PWM} falling
	Input high	V_{PWM_H}	2.4	–	–		V_{PWM} rising
	Input resistance	R_{IN-PWM}	3	5	7	kΩ	V_{PWM} = 1 V
	Open voltage	V_{PWM_O}	–	1.5	–	V	V_{PWM_O}
	Tri-state shutdown window[4]	V_{PWM_S}	1.2	–	1.9		–

[4] Maximum voltage range for tri-state

Table 11 Timing Characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
PWM tri-state to VSWH rising delay or VSWH falling delay	t_pts	–	15	–	ns	
VSWH Shutdown Hold-Off time	t_tsshd	–	150	–		
PWM to VSWH turn-off propagation delay	t_pdlu	–	20	–		
PWM to VSWH turn-on propagation delay	t_pdll	–	20	–		
DR_EN turn-off propagation delay falling	t_pdl_DR_EN	–	20	–		
DR_EN turn-on propagation delay rising	t_pdh_DR_EN	–	20	–		
PWM minimum pulse width	ton_min_PWM	–	25	–		
PWM minimum off time	toff_min_PWM	–	100	–		

5 Theory of Operation

The TDA21310 incorporates a high performance gate driver, one high-side power MOSFET and one low-side power MOSFET in a single 32 pin LG-UIQFN-32-2 package. The advantages of this arrangement are found in the areas of increased performance, increased efficiency and lower overall package and layout inductance. This module is ideal for use in Synchronous Buck Regulators.

The power MOSFETs are optimized for 5 V gate drive enabling excellent high load and light load efficiency. The gate driver is a robust high-performance driver rated at the switching node for DC voltages ranging from -1 V to +16 V. The power density for transmitted power in a multiphase regulator of this approach can easily be higher than 40 W per phase within a 25 mm^2 area.

5.1 Driver Characteristics

The gate driver of the TDA21310 has two input voltages, VCIN and VDRV. VCIN is the 5 V logic supply for the driver. VDRV sets the driving voltage for the high side and low side MOSFETs. The reference for the gate driver control circuit (VCIN) is CGND. To decouple the sensitive control circuitry (logic supply) from a noisy environment a ceramic capacitor must be placed between VCIN and CGND close to the pins. VDRV needs also to be decoupled using a ceramic capacitor (MLCC) between VDRV and PGND in close proximity to the pins. PGND serves as reference for the power circuitry including the driver output stage.

Referring to the Block Diagram page 7, VCIN is internally connected to the UVLO circuit. It will force shut-down for insufficient VCIN voltage. VDRV supplies the floating high-side drive – consisting of an active boot circuit - and the low-side drive circuit. A second UVLO circuitry, sensing the BOOT voltage level, is implemented to prevent false GH turn on during insufficient power supply level condition (BOOT cap charging/discharging sequence). During undervoltage both GH and GL are driven low actively; further passive pull-down (10 kΩ) is placed across gate-source of both FETs.

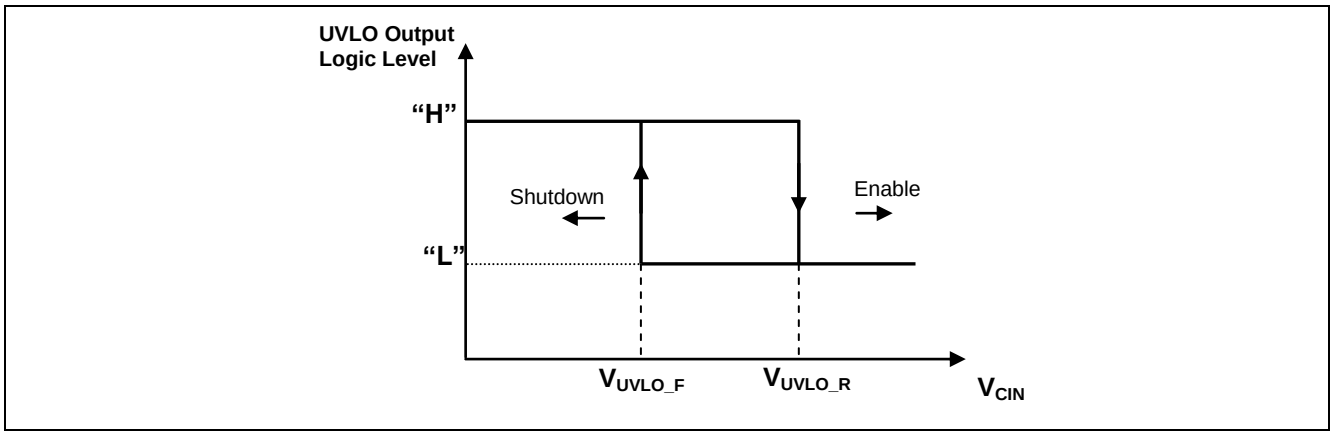


Figure 4 Internal Output Signal from UVLO Unit

5.2 Inputs to the Internal Control Circuits

The **PWM** is the control input to the IC from an external PWM controller and is compatible with 3.3 V.

The PWM input has tri-state functionality. When the voltage remains in the specified PWM-shutdown-window for at least the PWM-shutdown-holdoff time t_tsshd, the operation will be suspended by keeping both MOSFET gate outputs low. Once left open, the pin is held internally at a level of V_{PWM_O} = 1.5 V level.

Table 12 PWM Pin Functionality

PWM logic level	Driver output
Low	GL= High, GH = Low
High	GL = Low, GH = High
Open (left floating, or high impedance)	GL = Low, GH = Low

Using a wide range VCIN power supply (from 4.5 V to 6 V) causes a shifting in the threshold voltages for the following parameters: V_{PMW_O}, V_{PWM_H}, V_{PWM_L}. The typical behavior of these thresholds over VCIN voltage variation is shown in the following graph.

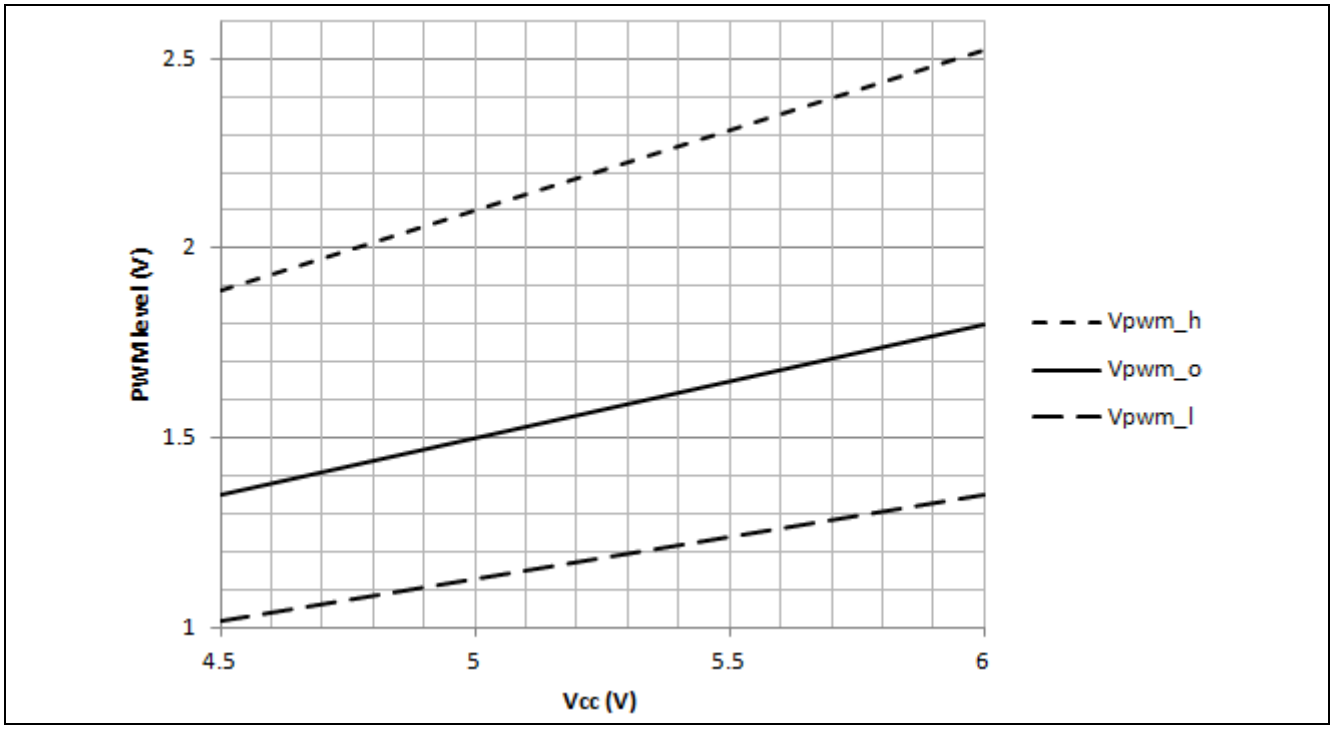


Figure 5 Variation of PWM levels versus VCIN logic supply voltage

Attention: The VPWM_S is also temperature dependent.

VCIN requires a minimum dv/dt of 300V/s in the vicinity of the UVLO threshold to prevent the driver logic from emitting any gate drive glitches.

The **DR_EN** is an active high signal. When DR_EN is pulled low, the power stage is disabled.

Table 13 DR_EN Pin Functionality

DR_EN logic level	Driver output
Low	Shutdown : GL = GH = Low
High	Enable : GL = GH = Active
Open (left floating, or high impedance)	Shutdown : GL = GH = Low

5.3 Shoot Through Protection

The TDA21310 driver includes gate drive functionality to protect against shoot through. In order to protect the power stage from overlap, both high-side and low-side MOSFETs being on at the same time, the adaptive control circuitry monitors specific voltages. When the PWM signal transitions to low, the high-side MOSFET will begin to turn off after the propagation delay time t_pdlu. When V_{GS} of the high-side MOSFET is discharged below 1 V (a threshold below which the high-side MOSFET is off), a secondary delay t_pdhl is initiated. After that delay the low-side MOSFET turns on regardless of the state of the “VSWH” pin. It ensures that the converter can sink current efficiently and the bootstrap capacitor will be refreshed appropriately during each switching cycle. See Figure 8 for more detail.

6 Application

6.1 Implementation

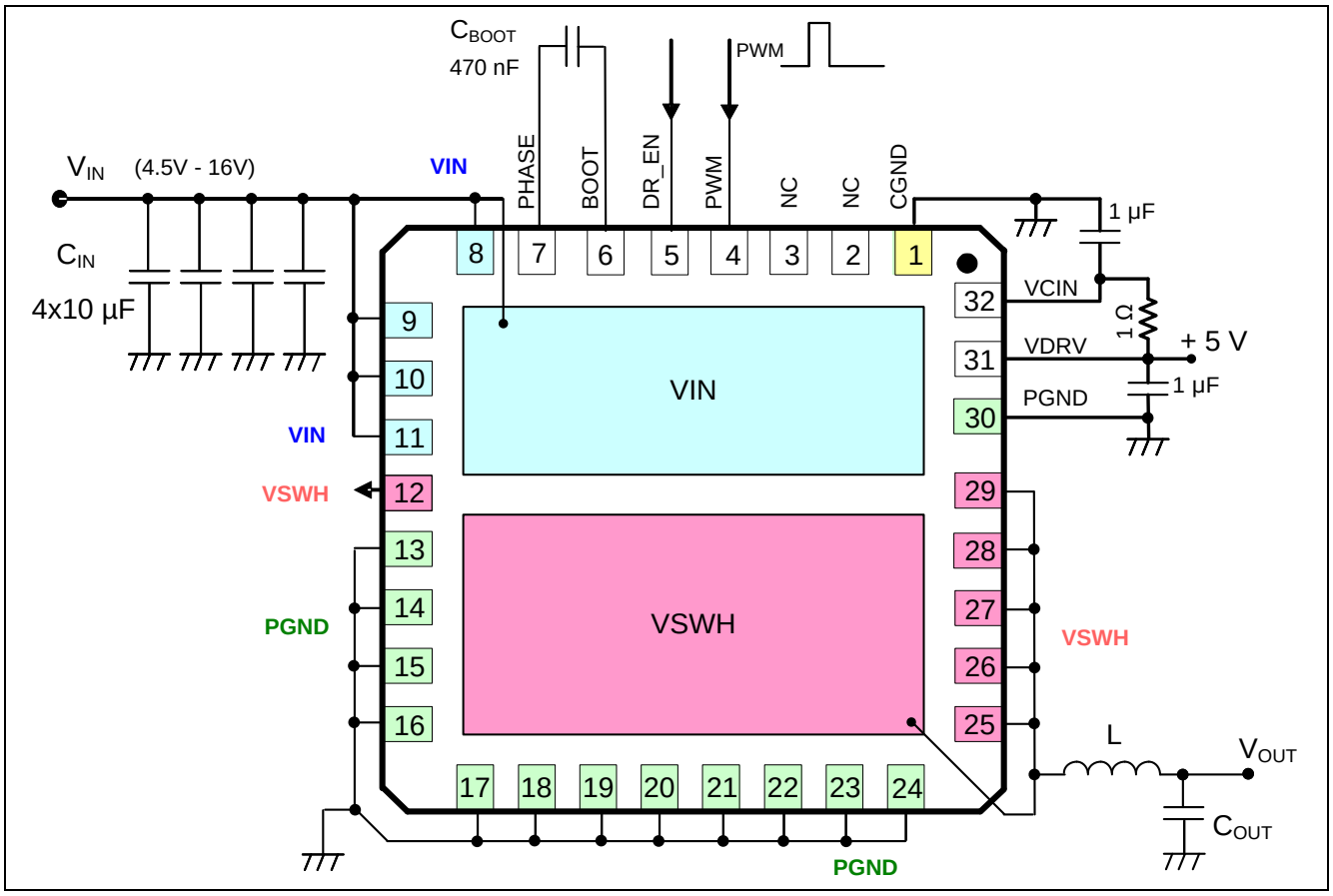


Figure 6 Pin interconnection outline (transparent top view)

Note:

1. *Pin PHASE is internally connected to VSWH node*
2. *It is recommended to place a RC filter between VCIN and VDRV as shown.*
3. *During power-up and down sequences, the PWM signal must be either low or tri-state (open voltage), but never high, in order to avoid uncontrolled output voltage.*

6.2 Typical Application

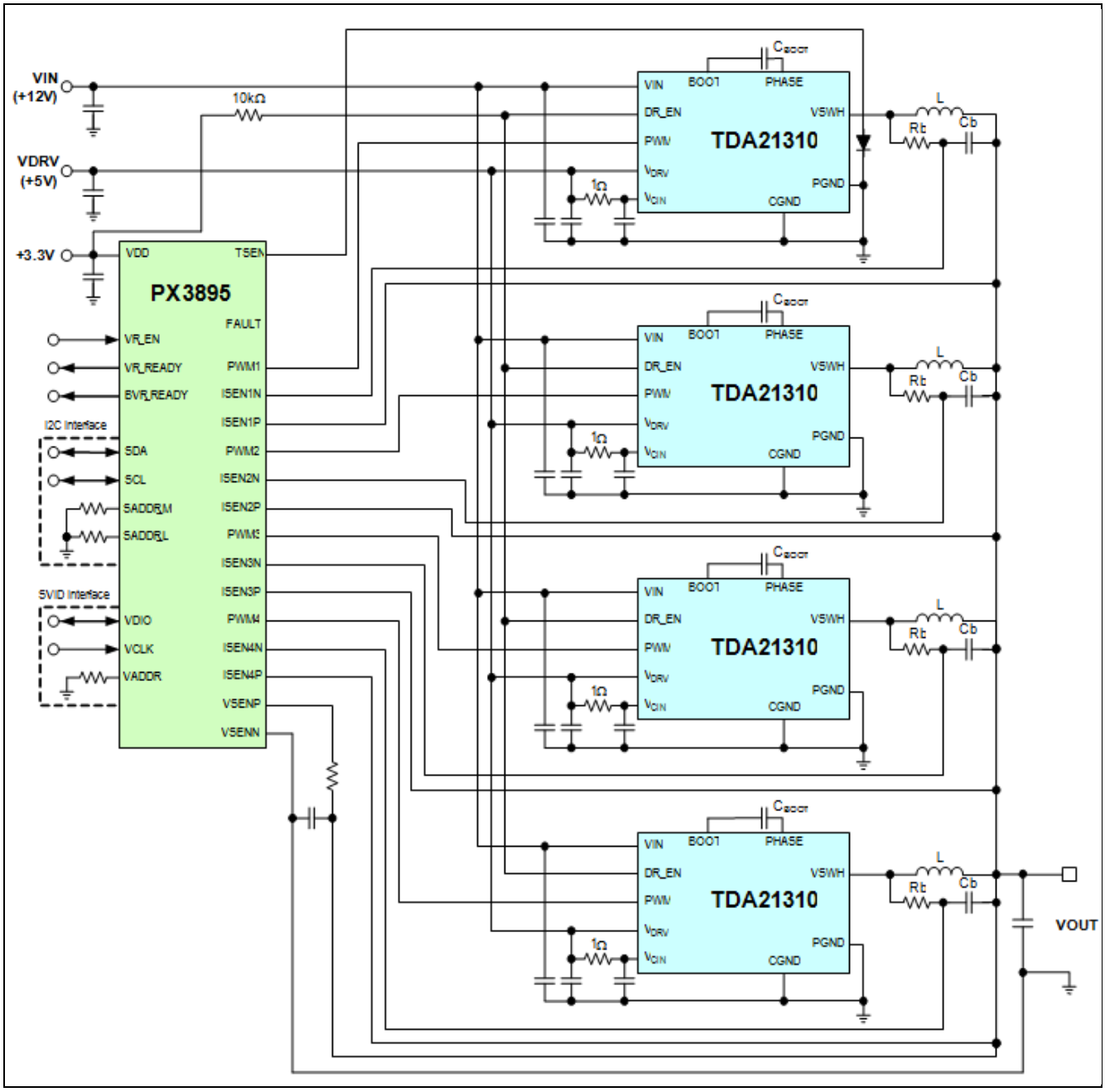


Figure 7 Four-phase voltage regulator - typical application (simplified schematic)

7 Gate Driver Timing Diagram

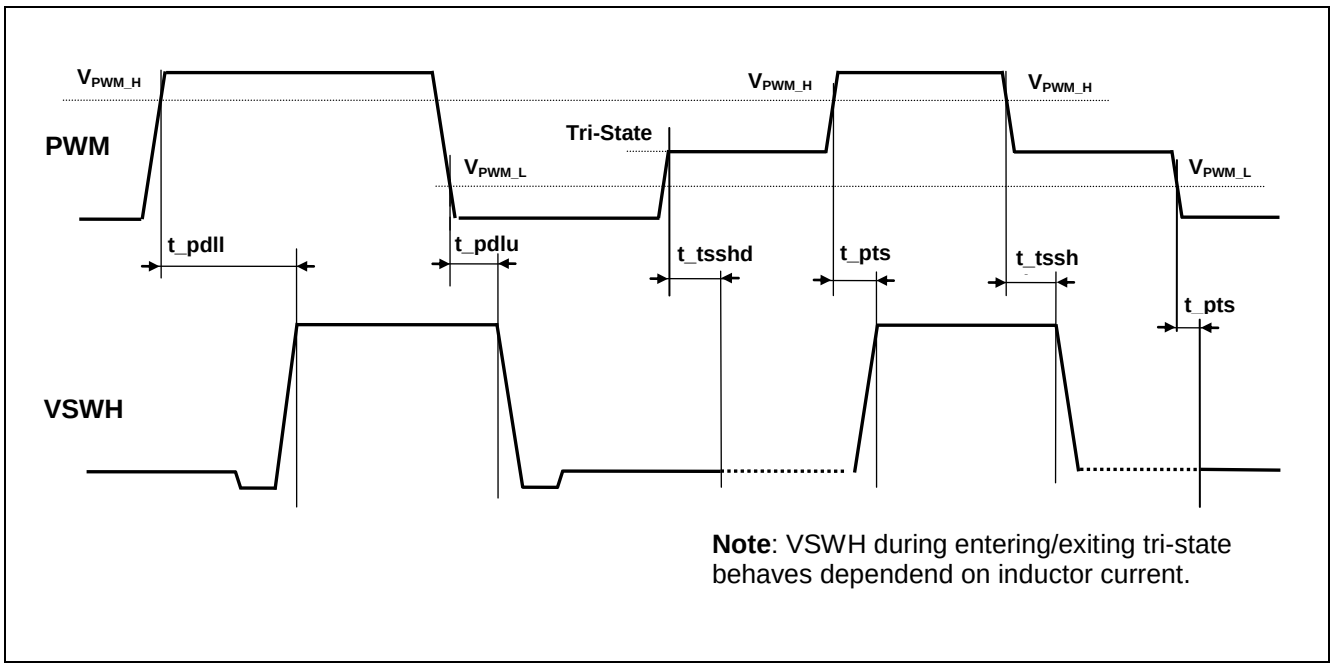


Figure 8 Adaptive gate driver timing diagram

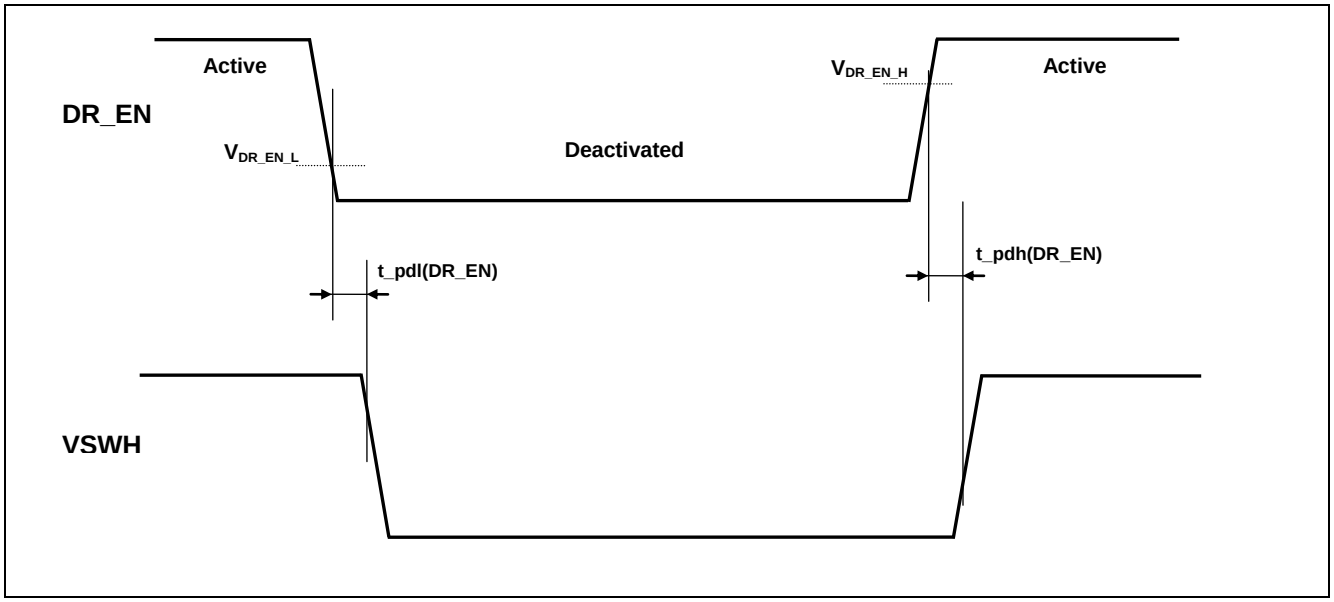


Figure 9 DR_EN timing diagram (PWM is assumed “high”)

8 Performance Curves – Typical Data

Operating conditions (unless otherwise specified): VIN = +12 V, VCIN = VDRV = +5 V, L_{OUT}=150nH (Cooper, FPI0906R1-R15, DCR = 0.29 mΩ) inductor, T_A = 25 °C, airflow = 300 LFM, no heatsink. Efficiency and power loss reported herein include only TDA21310 losses.

8.1 Temperature Rise

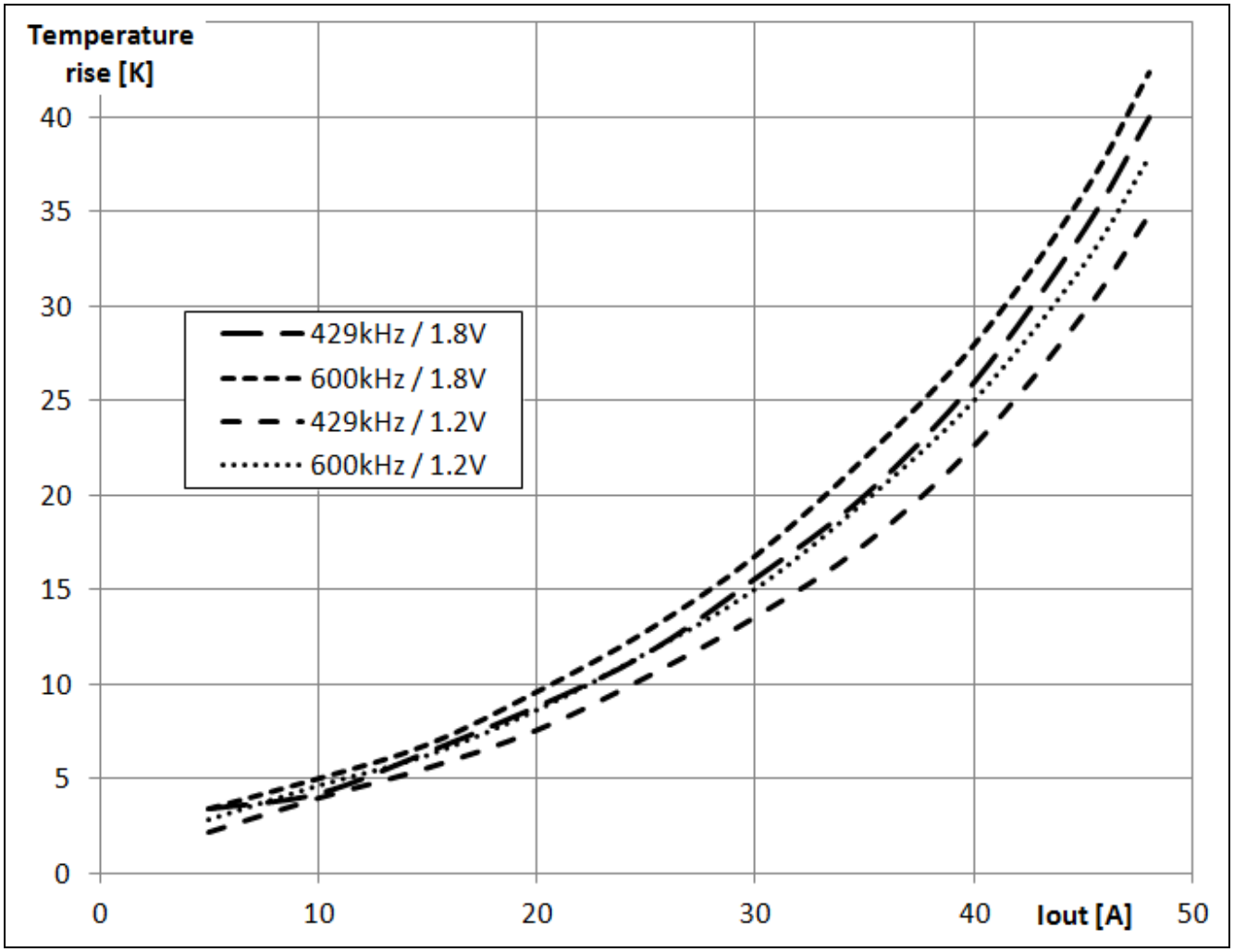


Figure 10 Temperature Rise over Output Current

8.2 Driver Current versus Switchig Frequency

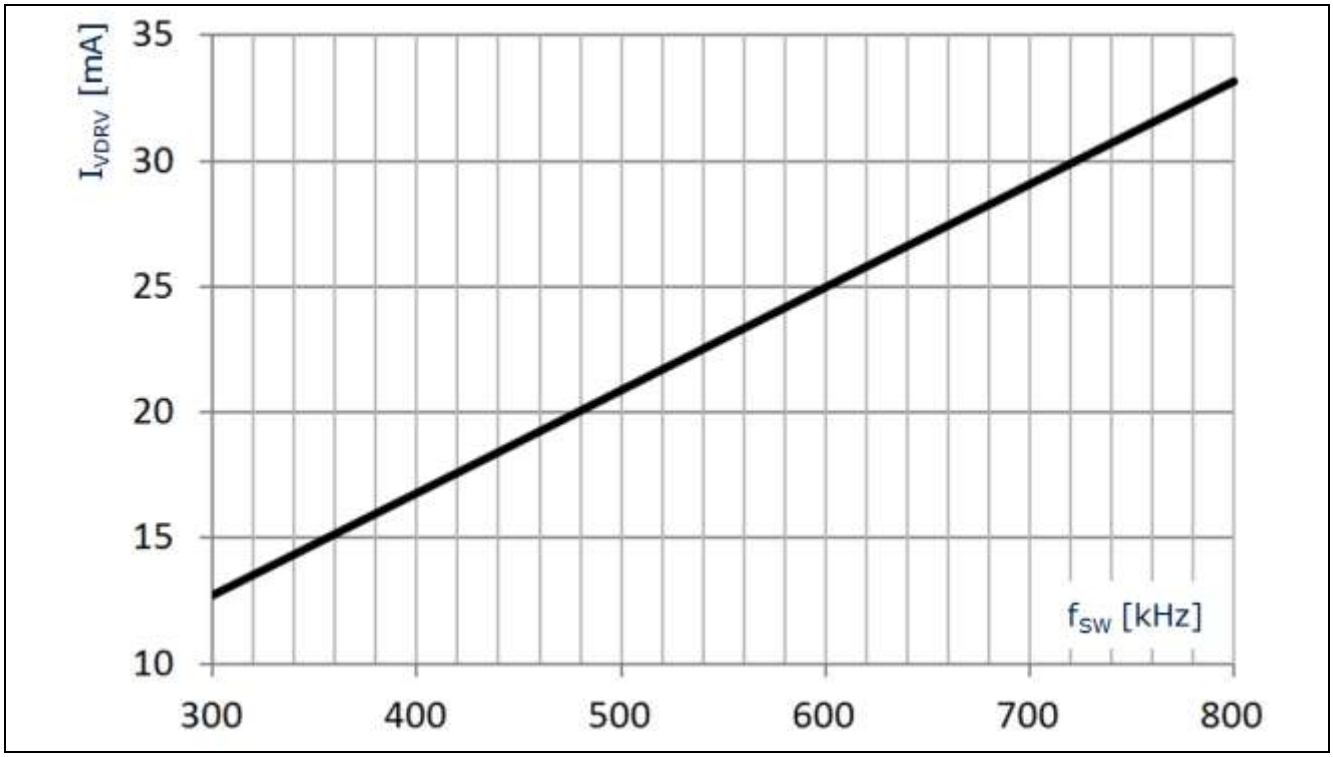


Figure 11 Driver Current over Switching Frequency in CCM Operation

8.3 Efficiency and Power Loss versus Switching Frequency

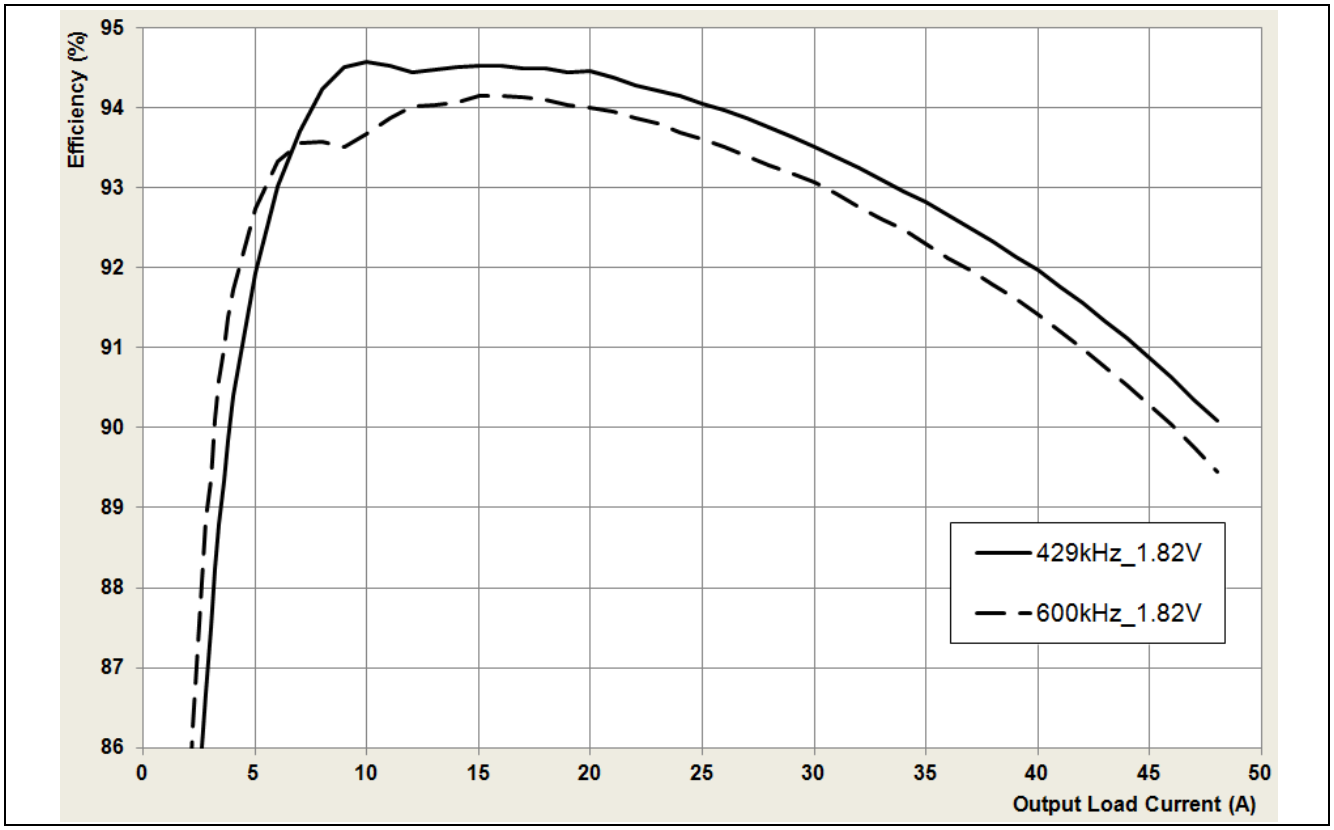


Figure 12 Efficiency at VIN = 12 V, VCIN = VDRV = 5 V, VOUT = 1.82 V, Parameter: f_{sw}

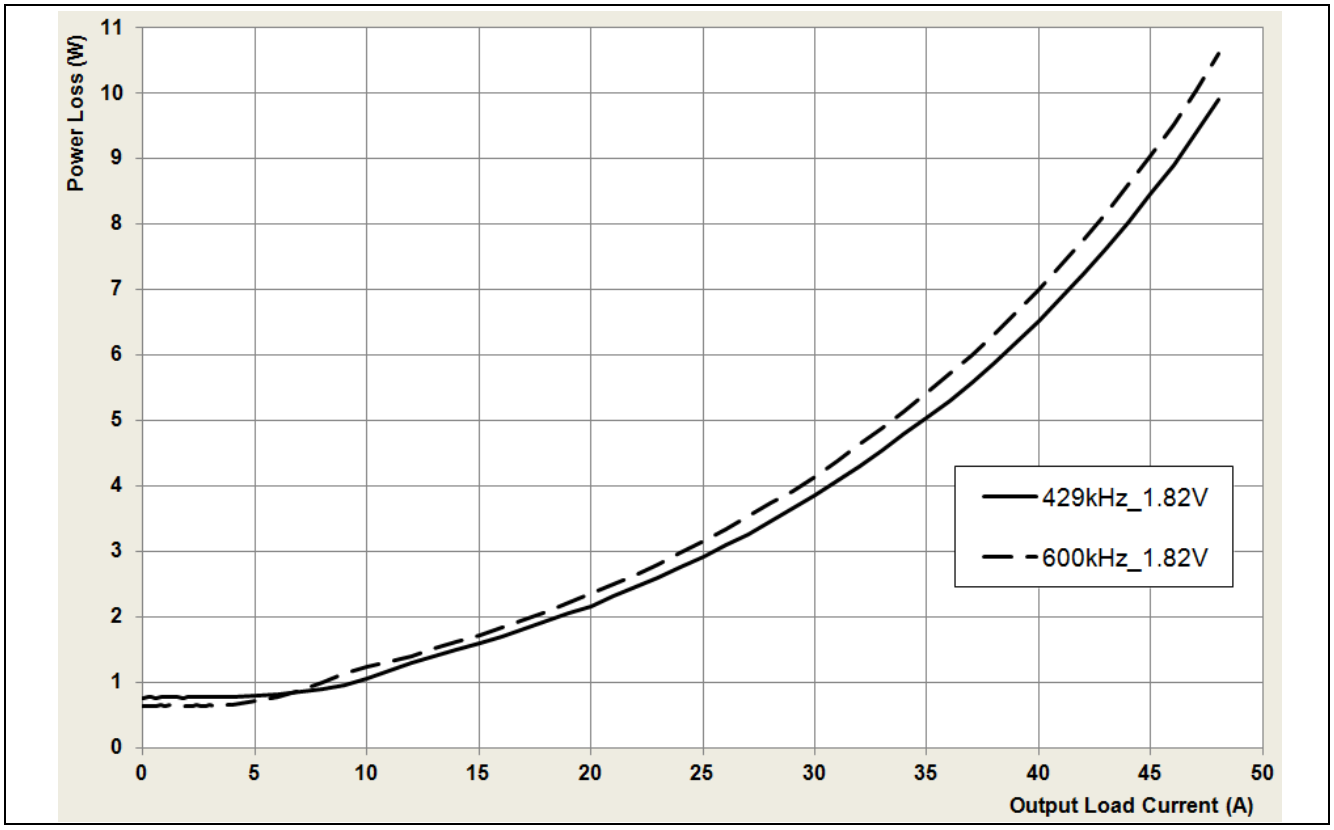


Figure 13 Power Loss at VIN = 12 V, VCIN = VDRV = 5 V, VOUT = 1.82 V, Parameter: f_{sw}

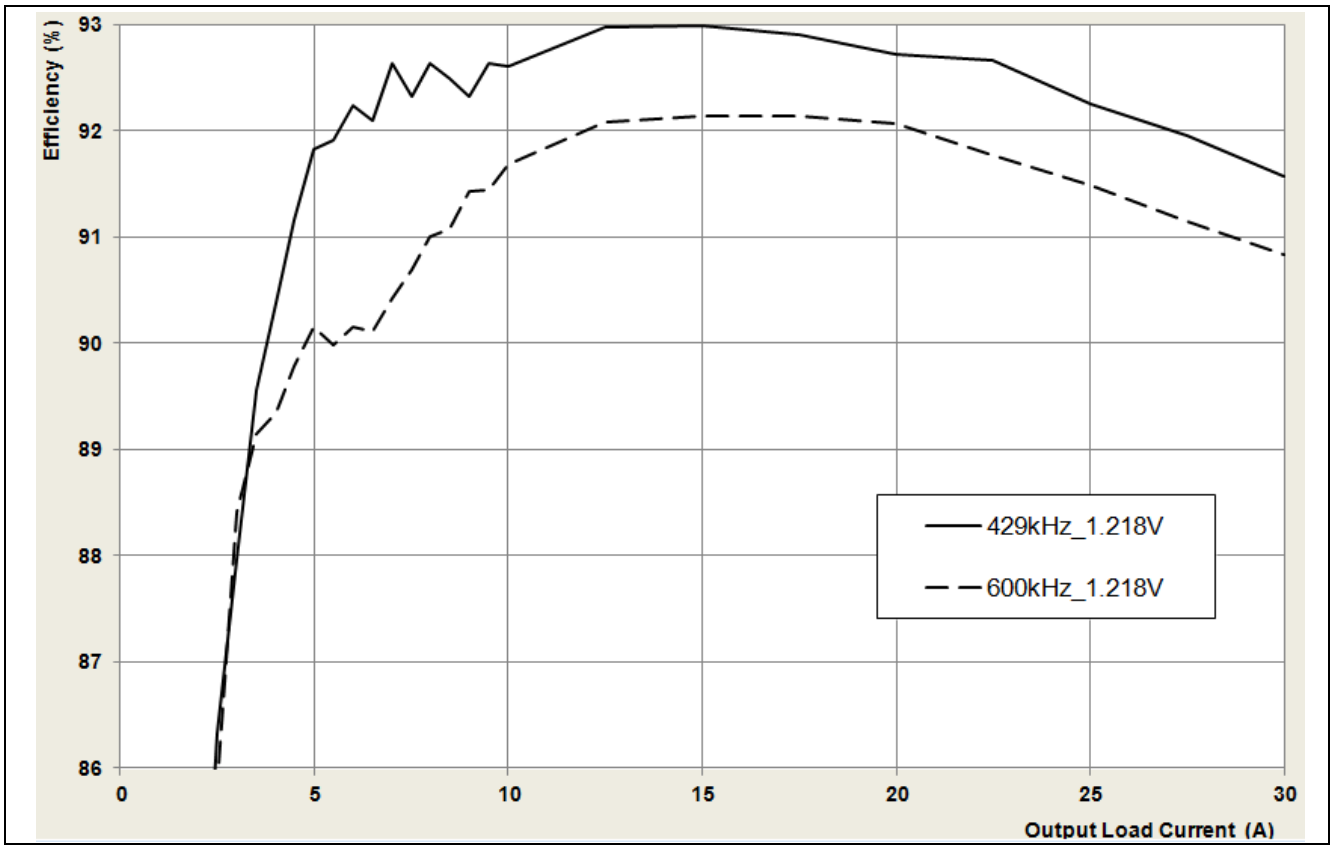


Figure 14 Efficiency at VIN = 12 V, VCIN = VDRV = 5 V, VOUT = 1.218 V, Parameter: f_{sw}

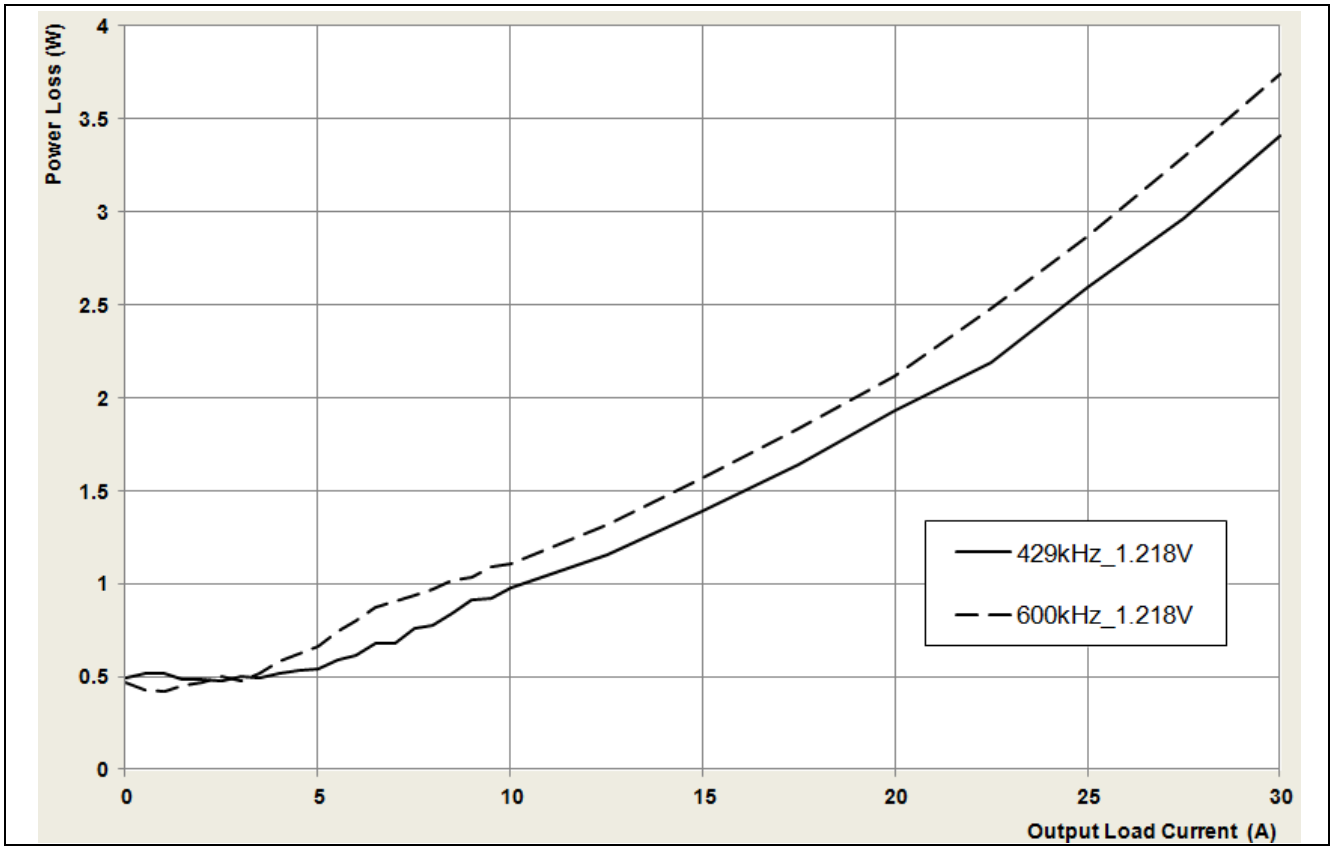
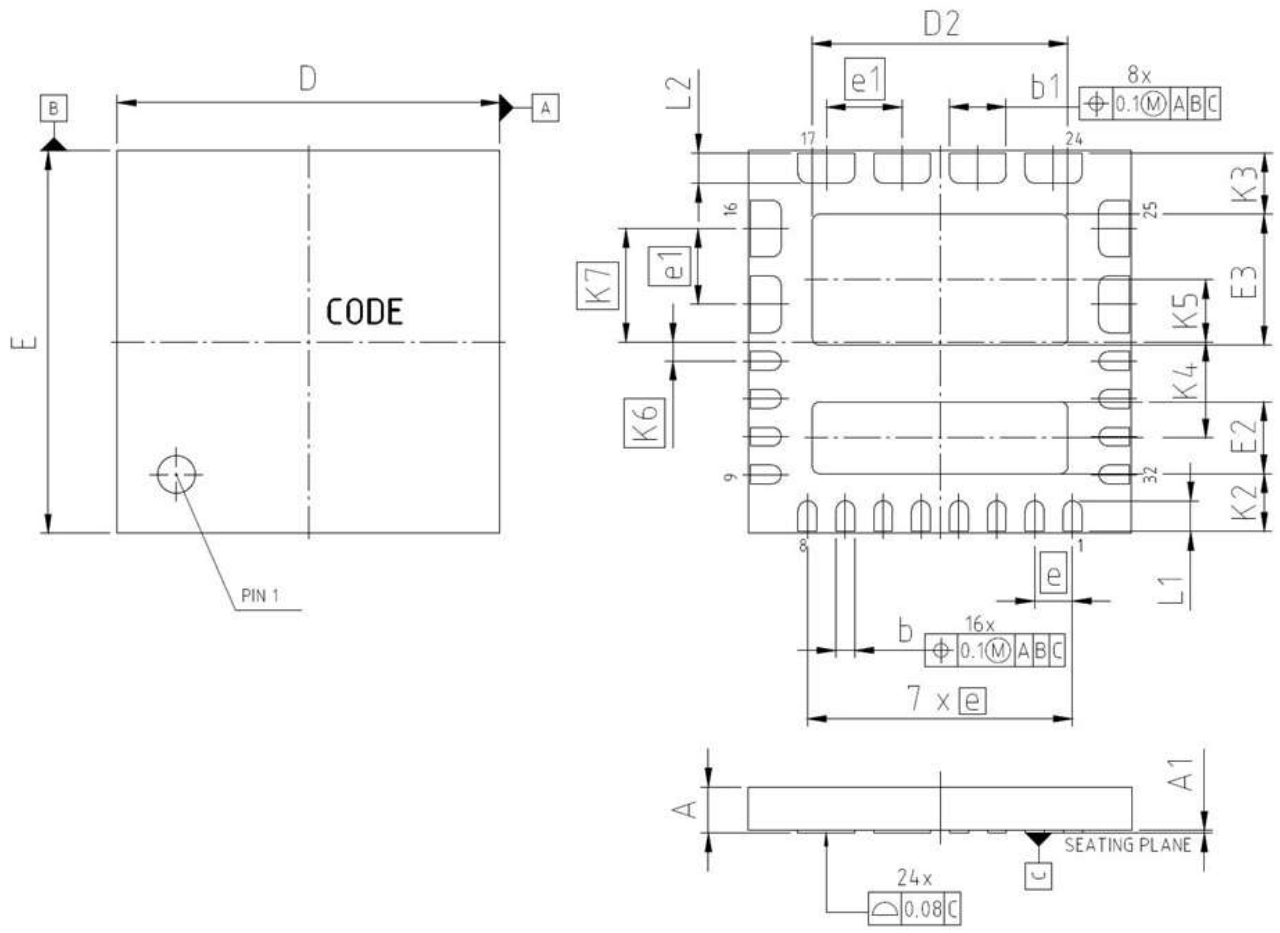


Figure 15 Power Loss at VIN = 12 V, VCIN = VDRV = 5 V, VOUT = 1.218 V, Parameter: f_{sw}

9 Mechanical Drawing LG-UIQFN-32-2



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	-	0.70	-	0.028
A1	-	0.05	-	0.002
b	0.20	0.30	0.008	0.012
b1	0.65	0.85	0.026	0.033
D	4.95	5.15	0.195	0.203
D2	3.28	3.48	0.129	0.137
e	0.50 (BSC)		0.020 (BSC)	
e1	1.00 (BSC)		0.039 (BSC)	
E	4.95	5.15	0.195	0.203
E2	0.85	1.05	0.033	0.041
E3	1.63	1.83	0.064	0.072
K2	0.66	0.86	0.026	0.034
K3	0.71	0.91	0.028	0.036
K4	1.17	1.37	0.046	0.054
K5	0.73	0.93	0.029	0.037
K6	0.25		0.010	
K7	1.50		0.059	
L1	0.33	0.47	0.013	0.019
L2	0.30	0.50	0.012	0.020

DOCUMENT NO.
Z8B00168222

SCALE
0 1.0 2mm

EUROPEAN PROJECTION

ISSUE DATE
08.02.2013

REVISION
01

Figure 16 Mechanical dimensions

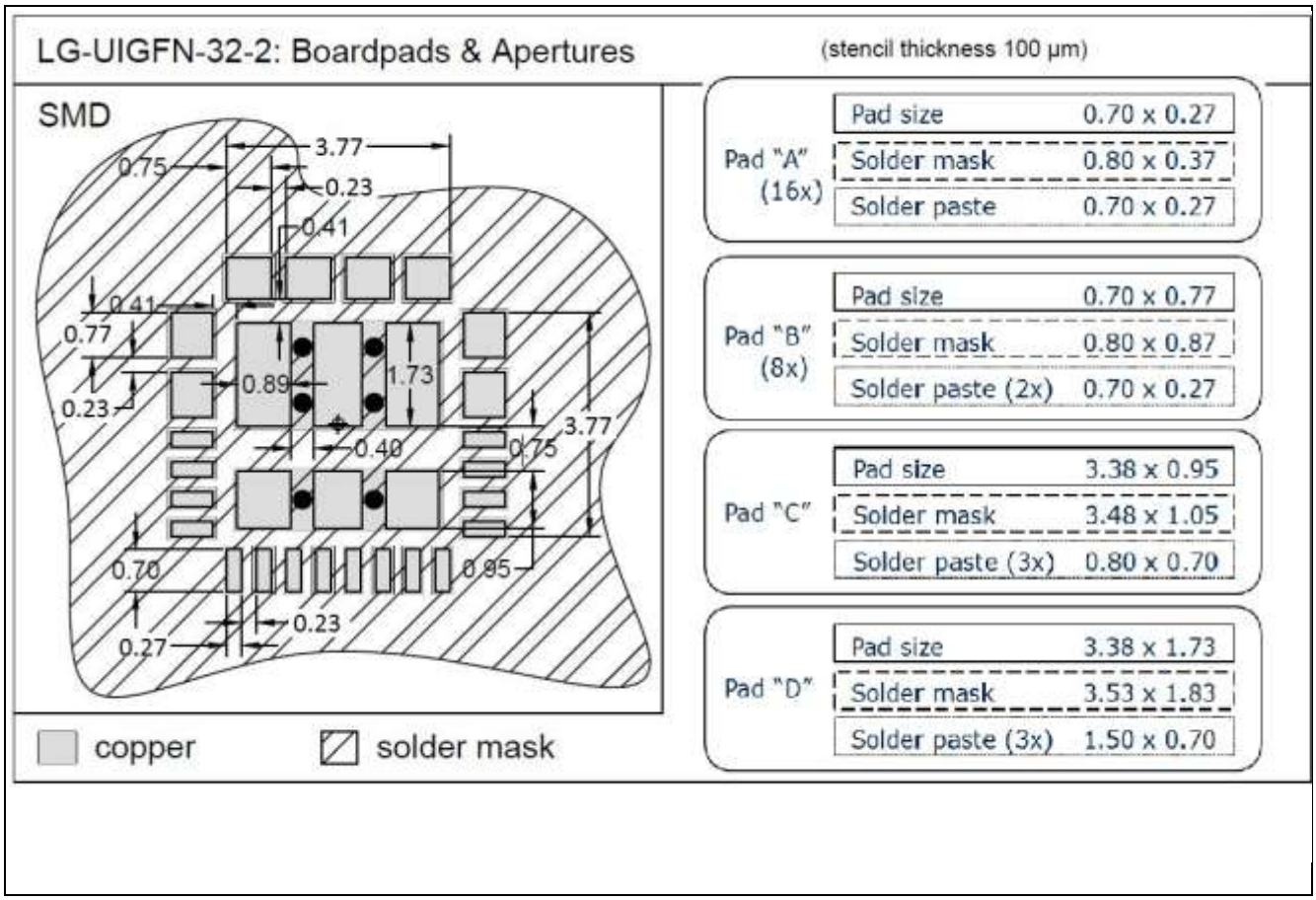


Figure 17 Stencil dimensions (in mm)

w w w . i n f i n e o n . c o m

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