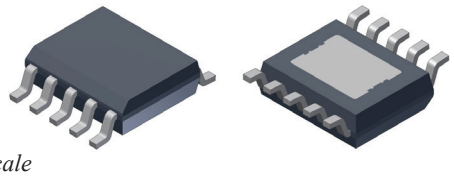
Wide Input Voltage, 2 A Buck Regulator Family with Low I_Q Mode

FEATURES AND BENEFITS

- Automotive AEC-Q100 qualified
- Withstands surge input to 40 V_{IN} for load dump
- Operates down to 3.4 V_{IN} (typ), 3.6 V_{IN} (max) for idle stop
- Utilizes pulse frequency modulation (PFM) for low I_Q mode
- Function options:
  - Selectable PWM / Low I_Q PFM mode, or
  - Selectable 10 µA Sleep mode (automatic PWM / Low I_Q PFM mode selection)
- Fixed output voltage options: 3.3 V or 5 V with ±1.0% accuracy
- Delivers up to 2 A of output current
- Integrated 110 mΩ high-side MOSFET
- Adjustable switching frequency from 300 to 550 kHz (to 605 kHz with sync)
- EMI Reduction Features:
  - Frequency dithering
  - Controlled switching node
- External synchronization capability
- Active low NPOR output with 7.5 ms delay

Continued on the next page…

PACKAGE: 10-pin SOIC with exposed thermal pad (suffix LK)



Not to scale

DESCRIPTION

The A8585 family is designed to provide the power supply requirements of next generation car audio and infotainment systems. The A8585 family provides all the control and protection circuitry to produce a high current regulator with ±1% output voltage accuracy.

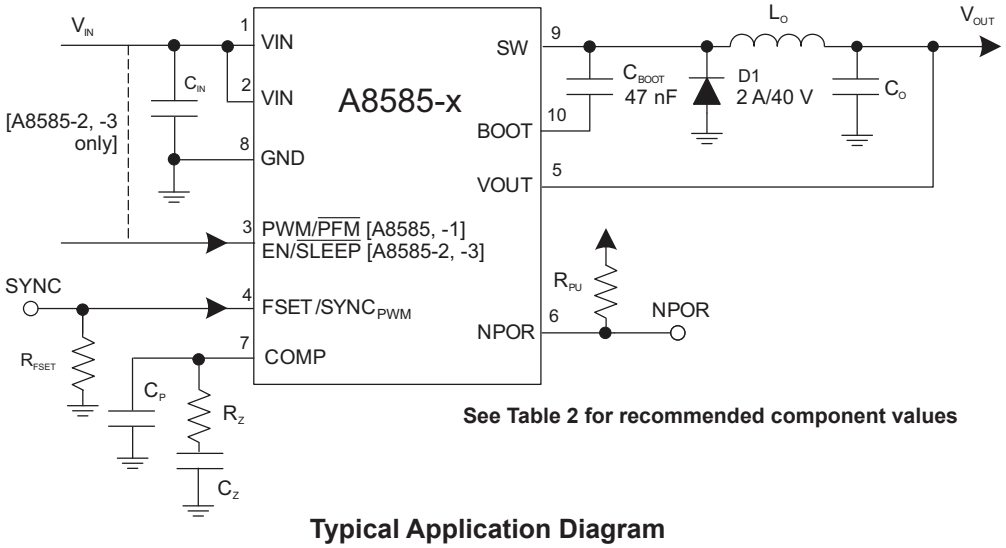
In PWM mode, the A8585 family employs current mode control to provide simple compensation, excellent stability, and fast transient response. In Low I_Q mode, the A8585 family employs pulse frequency modulation (PFM) to draw less than 33 µA from 12 V_{IN} while supplying 5 V/40 µA. When operational, the A8585 family operates down to at least 3.6 V_{IN} (V_{IN} falling). The selectable Sleep mode feature allows for very low standby current.

Features of the A8585 family include a programmable PWM switching frequency. The regulator switching frequency can be synchronized to an external clock. The A8585 has external compensation to optimize stability and transient response for a wide range of external components and applications. The A8585 has a fixed soft start time of 5 ms.

Continued on the next page…

APPLICATIONS:

- Automotive:
  - Instrument Clusters
  - Audio Systems
  - Navigation
  - HVAC
- Home audio
- Network and telecom
- Industrial



See Table 2 for recommended component values

Typical Application Diagram

FEATURES AND BENEFITS (continued)

- Pre-bias startup capable: V_{OUT} increases monotonically, will not cause a reset
- External compensation for maximum flexibility
- Stable with ceramic or electrolytic output capacitors
- Internally fixed soft start time of 5 ms
- Pulse-by-pulse current limit, hiccup mode short circuit, and thermal protections
- Pin open/short and component fault tolerant
- -40°C to 150°C operating junction temperature range
- Thermally enhanced SOIC-10 surface mount package

DESCRIPTION (continued)

Extensive protection features of the A8585 include pulse-by-pulse current limit, hiccup mode short circuit protection, open/short asynchronous diode protection, BOOT open/short voltage protection, V_{IN} undervoltage lockout, and thermal shutdown.

The A8585 is supplied in a 10-pin SOIC package (suffix LK) with exposed power pad. It is lead (Pb) free, with 100% matte-tin leadframe plating.

Selection Guide

Part Number	Packing*	Output Voltage Option	Function Option
A8585KLKTR-T	3000 pieces per 13-in. reel	5 V compatible	Selectable PWM / Low I_Q PFM
A8585KLKTR-T-1	3000 pieces per 13-in. reel	3.3 V compatible	
A8585KLKTR-T-2	Contact factory for availability	5 V compatible	Selectable Sleep (automatic PWM / Low I_Q PWM selection)
A8585KLKTR-T-3	Contact factory for availability	3.3 V compatible	

*Contact Allegro™ for additional packing options

Absolute Maximum Ratings*

Characteristic	Symbol	Notes	Rating	Unit
Input Voltage (VIN pins)	V_{IN}		–0.3 to 40	V
Switching Node Voltage (SW pin)	V_{SW}	Continuous; rating is a function of temperature	–0.3 to V_{IN} + 0.3	V
		t < 50 ns	–1.0 to V_{IN} + 3	V
BOOT Pin Voltage	V_{BOOT}	Continuous	V_{SW} – 0.3 to V_{SW} + 5.5	V
		BOOT pin overvoltage fault condition	V_{SW} – 0.3 to V_{SW} + 7	V
VOUT Pin Voltage	V_{OUT}	Continuous	–0.3 to 5.5	V
		VOUT pin overvoltage fault condition	–0.3 to 7	V
PWM/$\overline{\text{PFM}}$ Pin Voltage	$V_{PWM/\overline{PFM}}$	A8585, A8585-1	–0.3 to V_{IN} + 0.3	V
EN/$\overline{\text{SLEEP}}$ Pin Voltage	$V_{EN/\overline{SLEEP}}$	A8585-2, A8585-3	–0.3 to V_{IN} + 0.3	V
All other pins			–0.3 to 5.5	V
Maximum Junction Temperature	T_J(max)		150	ºC
Storage Temperature	T_{stg}		–55 to 150	ºC

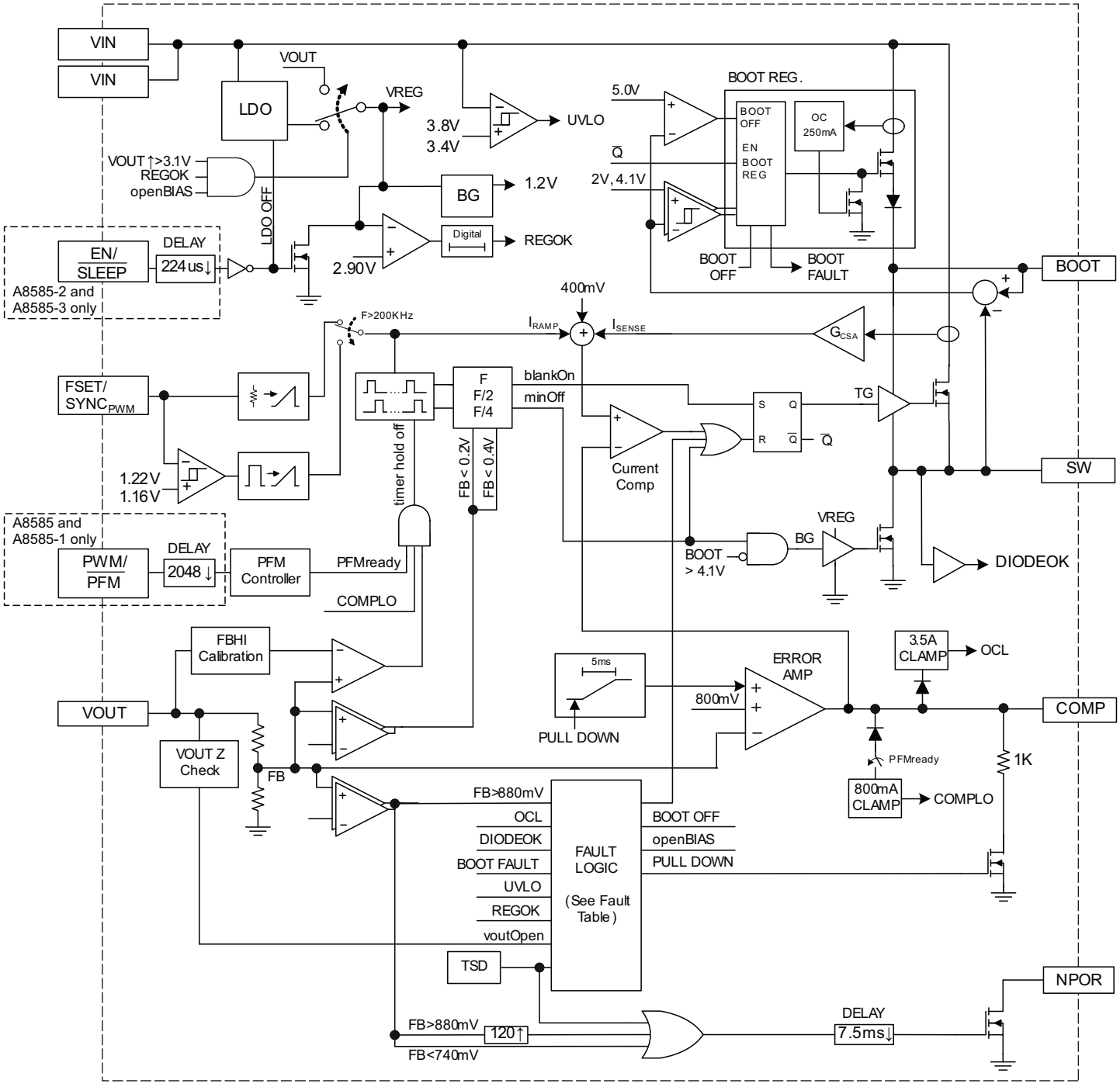
*Operation at levels beyond the ratings listed in this table may cause permanent damage to the device. The Absolute Maximum ratings are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the Electrical Characteristics table is not implied. Exposure to Absolute Maximum-rated conditions for extended periods may affect device reliability.

Thermal Characteristics: May require derating at maximum conditions; see Power Dissipation and Thermal Calculations section

Characteristic	Symbol	Test Conditions*	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	On 4-layer PCB based on JEDEC standard	35	°C/W

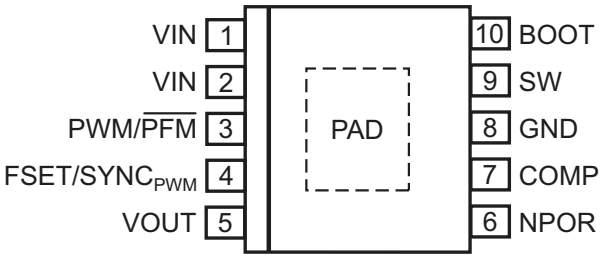
*Additional thermal information available on the Allegro website.

Table of Contents

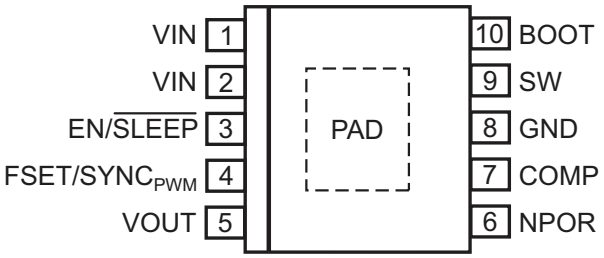


Functional Block Diagram

Pinout Diagrams



A8585 and A8585-1 variants



A8585-2 and A8585-3 variants

Terminal List Table

Number	Name	Function
1, 2	VIN	Power input for the control circuits and the drain of the internal high-side N-channel MOSFET. Connect this pin to a power supply of 4.0 to 35 V. A high quality, high frequency ceramic capacitor should be placed and grounded very close to this pin.
3	PWM/$\overline{\text{PFM}}$	(A8585 and A8585-1) Setting this pin high forces PWM mode. Setting this pin low allows Low I_Q PFM mode after 2048 clock cycles if two conditions are met: (1) the regulator is lightly loaded and (2) there is no clock signal being applied to the FSET/$SYNC_{PWM}$ input pin.
	EN/$\overline{\text{SLEEP}}$	(A8585-2 and A8585-3) This pin must be set high to enable the device. If this pin is set low, the device will enter a very low current shut down or sleep state (V_{OUT} = 0 V). If the application does not require a sleep mode, then this pin can be tied directly to VIN. Do not float this pin.
4	FSET/$SYNC_{PWM}$	Frequency setting and PWM synchronization pin. A resistor, R_{FSET}, from this pin to GND sets the PWM switching frequency. See figure 11 and/or equation 1 to determine the value of R_{FSET}. Applying a clock signal to this pin forces PWM mode (that is, it overrides a logic low on the PWM/$\overline{\text{PFM}}$ pin) and synchronizes the PWM switching frequency.
5	VOUT	Connect this pin to the output of the regulator. This pin supplies internal circuitry when its voltage level is high enough. Also, through an on-chip voltage divider, this pin connects to the negative feedback input of the error amplifier. Keep the VOUT pin quiet and kelvin connect.
6	NPOR	Active low, power on reset output signal. This pin is an open drain output that transitions from low to high impedance after the output has maintained regulation for t_{dPOR}.
7	COMP	Output of the error amplifier, and compensation node for the current mode control loop. Connect a series RC network from this pin to GND for loop compensation. See the Design and Component Selection section of this datasheet for further details.
8	GND	Ground pin.
9	SW	The source for the internal high-side N-channel MOSFET. The external free-wheeling diode (D_1) and output inductor (L_O) should be connected to this pin. Both D_1 and L_O should be placed close to this pin and connected with relatively wide traces.
10	BOOT	High-side gate drive boost input. This pin supplies the drive for the high-side N-channel MOSFET. Connect a 47 nF ceramic capacitor from BOOT to SW.
–	PAD	Exposed pad of the package providing enhanced thermal dissipation. This pad must be connected to the ground plane(s) of the PCB with at least 6 vias, directly in the pad.

ELECTRICAL CHARACTERISTICS[1]: Valid at 4.0 V ≤ V_{IN} ≤ 35 V, −40°C ≤ T_A = T_J ≤ 150°C, unless otherwise specified

Characteristic	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
Input Voltage							
Input Voltage Range[2]	V_{IN}			4.0	–	35	V
VIN Undervoltage Lockout Start Threshold	$V_{UVLO(ON)}$	V_{IN} rising		3.6	3.8	4.0	V
VIN Undervoltage Lockout Stop Threshold	$V_{UVLO(OFF)}$	V_{IN} falling		3.2	3.4	3.6	V
VIN Undervoltage Hysteresis	$V_{UVLO(HYS)}$			–	400	–	mV
Input Supply Current							
Input Supply Current (Not in PFM)	I_{IN}	I_{OUT} = 0 mA		–	2.5	3.5	mA
Input Supply Current (Low I_Q PFM) [3,4]	I_{LO_IQ} (0A,5.0V)	A8585	V_{IN} = 12 V, V_{OUT} = 5.0 V, $V_{PWM/\overline{PFM}}$ ≤ 1.2 V, I_{OUT} = No Load, T_A = 25°C	–	10	14	µA
			V_{IN} = 12 V, V_{OUT} = 5.0 V, $V_{PWM/\overline{PFM}}$ ≤ 1.2 V, I_{OUT} = No Load, T_A = 65°C	–	15	–	µA
	I_{LO_IQ} (40µA,5.0V)	A8585	V_{IN} = 12 V, V_{OUT} = 5.0 V, $V_{PWM/\overline{PFM}}$ ≤ 1.2 V, I_{OUT} = 40 µA, T_A = 25°C	–	28	33	µA
			V_{IN} = 12 V, V_{OUT} = 5.0 V, $V_{PWM/\overline{PFM}}$ ≤ 1.2 V, I_{OUT} = 40 µA, T_A = 65°C	–	33	–	µA
	I_{LO_IQ} (0A,3.3V)	A8585-1	V_{IN} = 12 V, V_{OUT} = 3.3 V, $V_{PWM/\overline{PFM}}$ ≤ 1.2 V, I_{OUT} = No Load, T_A = 25°C	–	7	10	µA
			V_{IN} = 12 V, V_{OUT} = 3.3 V, $V_{PWM/\overline{PFM}}$ ≤ 1.2 V, I_{OUT} = No Load, T_A = 65°C	–	12	–	µA
	I_{LO_IQ} (40µA,3.3V)	A8585-1	V_{IN} = 12 V, V_{OUT} = 3.3 V, $V_{PWM/\overline{PFM}}$ ≤ 1.2 V, I_{OUT} = 40 µA, T_A = 25°C	–	20	24	µA
			V_{IN} = 12 V, V_{OUT} = 3.3 V, $V_{PWM/\overline{PFM}}$ ≤ 1.2 V, I_{OUT} = 40 µA, T_A = 65°C	–	25	–	µA
Input Supply Current (Sleep Mode)	$I_{IN(SLEEP)}$	A8585-2 A8585-3	$V_{EN/\overline{SLEEP}}$ = 0 V, T_J ≤ 85°C, V_{IN} = 16 V	–	5	15	µA
			$V_{EN/\overline{SLEEP}}$ = 0 V, T_J ≤ 85°C, V_{IN} = 35 V	–	7	25	µA
Voltage Regulation							
Output Voltage Accuracy[5]	E_{VOUT} (5.0V)	A8585 A8585-2	0°C < T_J < 85°C, V_{OUT} = 4 × V_{COMP}	4.950	5.0	5.050	V
			–40°C < T_J < 150°C, V_{OUT} = 4 × V_{COMP}	4.925	5.0	5.075	V
	E_{VOUT} (3.3V)	A8585-1 A8585-3	0°C < T_J < 85°C, V_{OUT} = 2 × V_{COMP}	3.267	3.3	3.333	V
			–40°C < T_J < 150°C, V_{OUT} = 2 × V_{COMP}	3.250	3.3	3.350	V
Output Dropout Voltage[4]	$V_{O(PWM)}$	V_{IN} = 5.8 V, I_{OUT} = 1 A, f_{OSC} = 300 kHz		4.9	–	–	V
		V_{IN} = 6.3 V, I_{OUT} = 2 A, f_{OSC} = 300 kHz		4.9	–	–	V
Low I_Q Mode Ripple[3,4]	$V_{PP(LO\_IQ)}$	8 V < V_{IN} < 12 V		–	25	65	mV_{PP}
Low I_Q Peak Current Threshold	$I_{PEAK(LO\_IQ)}$			640	800	930	mA_{PEAK}

Continued on the next page…

[1]Negative current is defined as coming out of the node or pin, positive current is defined as going into the node or pin.
[2]Thermally limited depending on input voltage, output voltage, duty cycle, regulator load currents, PCB layout, and airflow.
[3]Configured as shown in Typical Application diagram.
[4]Ensured by design and characterization, not production tested.
[5]At 0°C < T_J < 85°C, ensured by design and characterization, not production tested.

ELECTRICAL CHARACTERISTICS[1] (continued): Valid at 4.0 V ≤ V_{IN} ≤ 35 V, −40°C ≤ T_A = T_J ≤ 150ºC, unless otherwise specified

Characteristic	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
Error Amplifier							
Open Loop Voltage Gain	A_{VOL}	V_{COMP} = 1.2 V		–	65	–	dB
Transconductance with On-Chip Resistor Divider Included	$g_{m(5.0V)}$	A8585 A8585-2	2.5 V < V_{OUT}	88.0	120.0	152.0	µA/V
			0 V < V_{OUT} < 2.5 V	46.4	64.0	81.6	µA/V
	$g_{m(3.3V)}$	A8585-1 A8585-3	1.65 V < V_{OUT}	133.3	181.8	230.3	µA/V
			0 V < V_{OUT} < 1.65 V	70.3	97.0	123.6	µA/V
Output Current	I_{EA}	V_{COMP} = 1.2 V		–	±75	–	µA
Internal MOSFET Parameters[2]							
High-Side MOSFET[4]	$R_{DS(on)HS}$	T_J = 25ºC, V_{BOOT} – V_{SW} = 4.5 V, I_{DS} = 1.0 A		–	110	130	mΩ
High-Side MOSFET Leakage[5]	I_{LKGHS}	T_J < 85ºC, $V_{EN/\overline{SLEEP}}$ ≤ 0.8 V, V_{SW} = 0 V, V_{IN} = 16 V		–	–	10	µA
		T_J ≤ 150ºC, $V_{EN/\overline{SLEEP}}$ ≤ 0.8 V, V_{SW} = 0 V, V_{IN} = 16 V		–	60	150	µA
SW Node Rising/Falling Slew Rate[4]	SR	V_{IN} = 12 V, I_{OUT} = 1 A		–	0.72	–	V/ns
Low-Side MOSFET	$R_{DS(on)LS}$	T_J = 25ºC, V_{IN} ≥ 6 V, I_{DS} = 0.1 A		–	–	10	Ω
BOOT Regulator							
BOOT Voltage Enable Threshold	$V_{BOOT(TH)}$	V_{BOOT} rising		1.8	2.0	2.2	V
BOOT Voltage Enable Hysteresis	$V_{BOOT(HYS)}$			–	400	–	mV
Oscillator and PWM Timing							
PWM Switching Frequency	f_{OSC}	R_{FSET} = 86.6 kΩ		270	300	330	KHz
		R_{FSET} = 61.9 kΩ		373	415	457	KHz
		R_{FSET} = 45.3 kΩ		495	550	605	KHz
PWM Frequency Dithering	f_{DITHER}	No dithering with synchronization		–	±7.5	–	%
Minimum Controllable On-Time	$t_{ON(MIN)}$	V_{IN} = 12 V, I_{OUT} = 1 A		–	100	140	ns
Minimum Switch Off-Time	$t_{OFF(MIN)}$	V_{IN} = 12 V, I_{OUT} = 1 A		–	135	160	ns
FSET/SYNC$_{PWM}$ Synchronization Timing							
Synchronization Frequency Range	f_{SW_MULT}			375	–	605	KHz
Synchronization Input Duty Cycle	D_{SYNC}			–	–	80	%
Synchronization Input Pulse Width	t_{wSYNC}			200	–	–	ns
Synchronization Input Rise Time[4]	t_{rSYNC}			–	10	15	ns
Synchronization Input Fall Time[4]	t_{fSYNC}			–	10	15	ns
Synchronization Rising Threshold[4]	$V_{SYNC\ LO}$	$V_{FSET/SYNCPWM}$ Rising		–	–	1.5	V
Synchronization Falling Threshold[4]	$V_{SYNC\ HI}$	$V_{FSET/SYNCPWM}$ Falling		0.9	–	–	V

Continued on the next page…

[1]Negative current is defined as coming out of the node or pin, positive current is defined as going into the node or pin.
[2]Thermally limited depending on input voltage, output voltage, duty cycle, regulator load currents, PCB layout, and airflow.
[3]Configured as shown in Typical Application diagram.
[4]Ensured by design and characterization, not production tested.
[5]At 0ºC < T_J < 85ºC, ensured by design and characterization, not production tested.

ELECTRICAL CHARACTERISTICS[1] (continued): Valid at 4.0 V ≤ V_{IN} ≤ 35 V, −40°C ≤ T_A = T_J ≤ 150ºC, unless otherwise specified

Characteristic	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
Current Control Loop							
PWM Pulse-by-Pulse Limit	$I_{LIM(TONMIN)}$	$t_{ON} = t_{ON(MIN)PWM}$		3.0	3.5	4.0	A
	$I_{LIM(TONMAX)}$	$t_{ON} = (1/f_{SW}) - t_{OFF(MIN)PWM}$, no PWM synchronization		2.0	2.6	3.0	A
COMP to SW Current Gain	g_{mPOWER}			–	3	–	A/V
Slope Compensation	S_E	During synchronization		–	0.35	–	A/µs
		R_{FSET} = 86.6 kΩ		0.18	0.25	0.34	A/µs
		R_{FSET} = 61.9 kΩ		0.25	0.34	0.45	A/µs
		R_{FSET} = 45.3 kΩ		0.34	0.45	0.58	A/µs
Soft Start							
Soft Start Ramp Time	t_{SS}			2.5	5.0	7.5	ms
Soft Start Switching Frequency	$f_{SS(5.0V)}$	A8585 A8585-2	0 V < V_{OUT} < 1.25 V	–	$f_{OSC}/4$	–	kHz
			1.25 V < V_{OUT} < 2.5 V		$f_{OSC}/2$		kHz
			2.5 V < V_{OUT}	–	f_{OSC}	–	kHz
	$f_{SS(3.3V)}$	A8585-1 A8585-3	0 V < V_{OUT} < 0.825 V	–	$f_{OSC}/4$	–	kHz
			0.825 V < V_{OUT} < 1.65 V		$f_{OSC}/2$		kHz
			1.65 V < V_{OUT}	–	f_{OSC}	–	kHz
Hiccup Mode							
Hiccup Off-Time	HIC_{OFF}	All hiccup faults such as VOUT shorted to GND		–	20	–	ms
Hiccup Overcurrent Protection (OCP) Count	OCP_{LIM}	t > t_{SS}, OCP pulses		–	120	–	counts
Hiccup BOOT Shorted Count	$BOOT_{UV}$			–	64	–	counts
Hiccup BOOT Open Count	$BOOT_{OV}$			–	7	–	counts
PWM/$\overline{\text{PFM}}$ Pin Input Thresholds							
PWM Threshold (High)	V_{IH}	A8585	4.5 V < V_{OUT} < 5.5 V, $V_{PWM/\overline{PFM}}$ rising	–	–	2.6	V
		A8585-1	3.0 V < V_{OUT} < 3.6 V, $V_{PWM/\overline{PFM}}$ rising	–	–	2.0	V
PFM Threshold (Low)	V_{IL}	A8585	4.5 V < V_{OUT} < 5.5 V, $V_{PWM/\overline{PFM}}$ falling	1.2	–	–	V
		A8585-1	3.0 V < V_{OUT} < 3.6 V, $V_{PWM/\overline{PFM}}$ falling	0.8	–	–	V
PWM/$\overline{\text{PFM}}$ Hysteresis	V_{HYS}	A8585	4.5 V < V_{OUT} < 5.5 V, $V_{IH} - V_{IL}$	–	400	–	mV
		A8585-1	3.0 V < V_{OUT} < 3.6 V, $V_{IH} - V_{IL}$	–	200	–	mV
PWM/$\overline{\text{PFM}}$ Pin Input Resistance	R_{IN}	A8585, A8585-1		120	200	280	kΩ
PWM/$\overline{\text{PFM}}$ Turn-Off Delay	t_{dLO_IQ}	A8585, A8585-1	From PWM/PFM transitioning low, or NPOR transitioning high, to start Low I_Q mode	–	2048	–	counts

Continued on the next page…

[1]Negative current is defined as coming out of the node or pin, positive current is defined as going into the node or pin.
[2]Thermally limited depending on input voltage, output voltage, duty cycle, regulator load currents, PCB layout, and airflow.
[3]Configured as shown in Typical Application diagram.
[4]Ensured by design and characterization, not production tested.
[5]At 0ºC < T_J < 85ºC, ensured by design and characterization, not production tested.

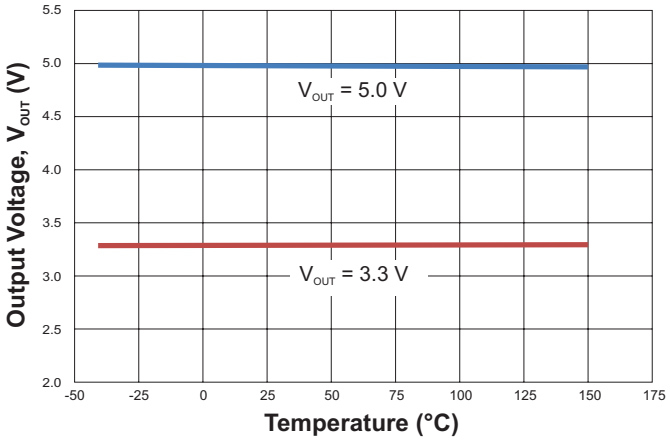
ELECTRICAL CHARACTERISTICS[1] (continued): Valid at 4.0 V ≤ V_{IN} ≤ 35 V, −40°C ≤ T_A = T_J ≤ 150ºC, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Thermal Protection						
Thermal Shutdown Threshold (Rising)	T_{SDth}	PWM stops immediately, COMP is pulled low, and soft start is reset	155	170	–	ºC
Thermal Shutdown Hysteresis	T_{SDHYS}		–	20	–	ºC
Power On Reset (NPOR) Output						
NPOR Overvoltage Threshold, 5.0V	$V_{NPOROV(5.0V)}$	V_{OUT} rising	5.37	5.5	5.75	V
NPOR Overvoltage Hysteresis, 5.0V	$V_{NPOROV(HYS)(5.0V)}$	V_{OUT} falling, relative to V_{NPOROV}	–	-60	–	mV
NPOR Undervoltage Threshold, 5.0V	$V_{NPORUV(5.0V)}$	V_{OUT} falling	4.45	4.62	4.75	V
NPOR Undervoltage Hysteresis, 5.0V	$V_{NPORUV(HYS)(5.0V)}$	V_{OUT} rising, relative to V_{NPORUV}	–	60	–	mV
NPOR Overvoltage Threshold, 3.3V	$V_{NPOROV(3.3V)}$	V_{OUT} rising	3.54	3.63	3.75	V
NPOR Overvoltage Hysteresis, 3.3V	$V_{NPOROV(HYS)(3.3V)}$	V_{OUT} falling, relative to V_{NPOROV}	–	-40	–	mV
NPOR Undervoltage Threshold, 3.3V	$V_{NPORUV(3.3V)}$	V_{OUT} falling	2.93	3.05	3.14	V
NPOR Undervoltage Hysteresis, 3.3V	$V_{NPORUV(HYS)(3.3V)}$	V_{OUT} rising, relative to V_{NPORUV}	–	40	–	mV
NPOR Overvoltage Delay	t_{dPOV_POR}	V_{OUT} falling beyond V_{NPOROV}	–	120	–	counts
NPOR Delay to Rising Edge	t_{dPOR}	V_{OUT} rising only	5	7.5	10	ms
NPOR Low Output Voltage	V_{POROL}	I_{NPOR} = 4 mA	–	200	400	mV
NPOR Leakage	I_{LKGPOR}	V_{NPOR} = 5.5 V	–	–	1.2	µA
EN/$\overline{\text{SLEEP}}$ Pin Input Thresholds						
EN/$\overline{\text{SLEEP}}$ Threshold (High)	$V_{SLEEPVIH}$	A8585-2 A8585-3 $V_{EN/\overline{SLEEP}}$ rising	–	1.3	2.1	V
EN/$\overline{\text{SLEEP}}$ Threshold (Low)	$V_{SLEEPVIL}$	A8585-2 A8585-3 $V_{EN/\overline{SLEEP}}$ falling	0.5	1.2	–	V
EN/$\overline{\text{SLEEP}}$ Delay	t_{dSLEEP}	A8585-2 A8585-3 $V_{EN/\overline{SLEEP}}$ transitioning low	115	224	400	µs
EN/$\overline{\text{SLEEP}}$ Input Bias Current	$I_{BIASSLEEP}$	A8585-2 A8585-3 $V_{EN/\overline{SLEEP}}$ = 5 V	–	500	–	nA

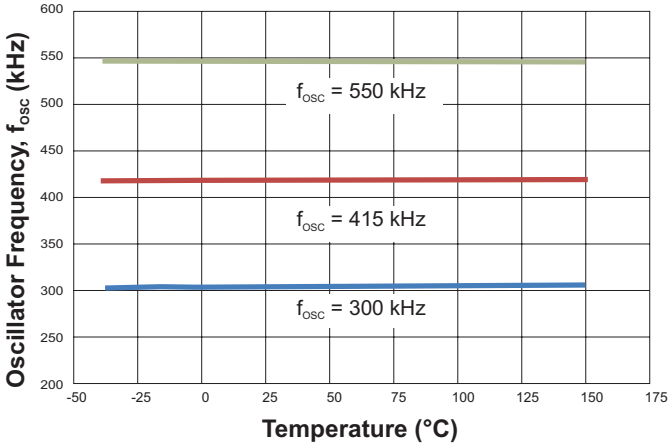
[1]Negative current is defined as coming out of the node or pin, positive current is defined as going into the node or pin.
[2]Thermally limited depending on input voltage, output voltage, duty cycle, regulator load currents, PCB layout, and airflow.
[3]Configured as shown in Typical Application diagram.
[4]Ensured by design and characterization, not production tested.
[5]At 0ºC < T_J < 85ºC, ensured by design and characterization, not production tested.

CHARACTERISTIC PERFORMANCE

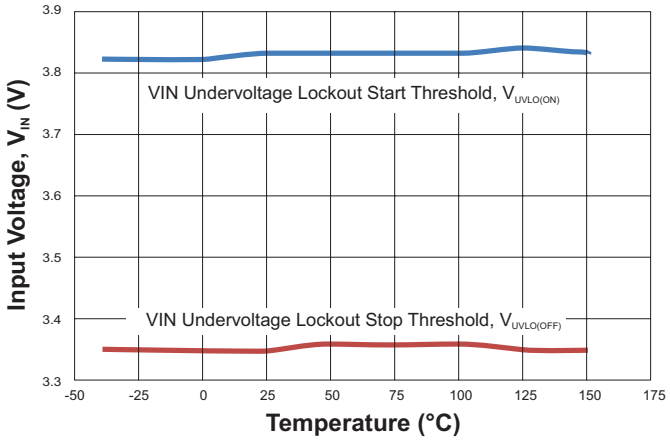
Output Voltage versus Temperature



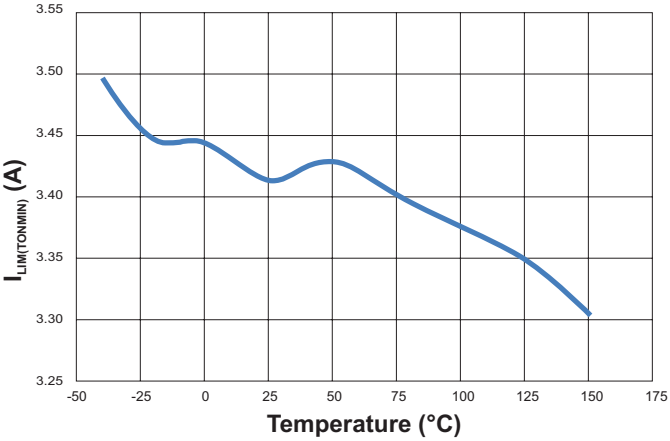
Switching Frequency versus Temperature



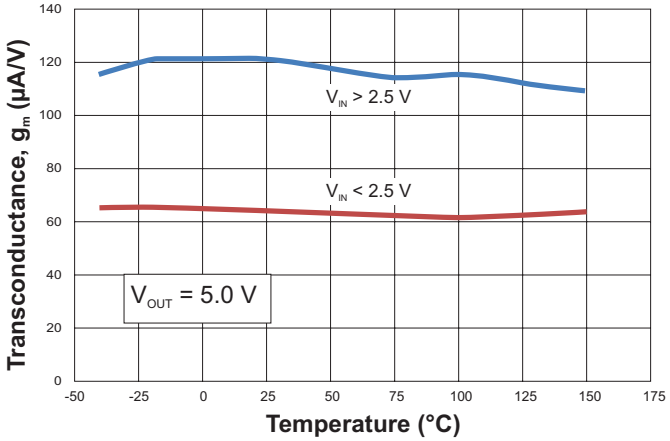
VIN UVLO Start and Stop Thresholds versus Temperature



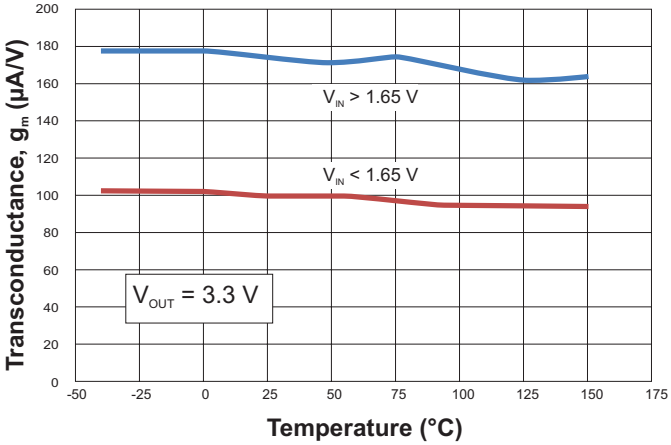
Pulse-by-Pulse Current Limit at $t_{ON(MIN)}$ versus Temperature



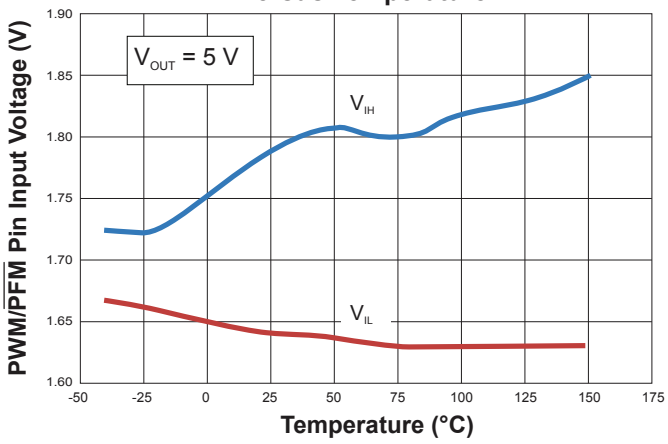
Error Amplifier Transconductance versus Temperature



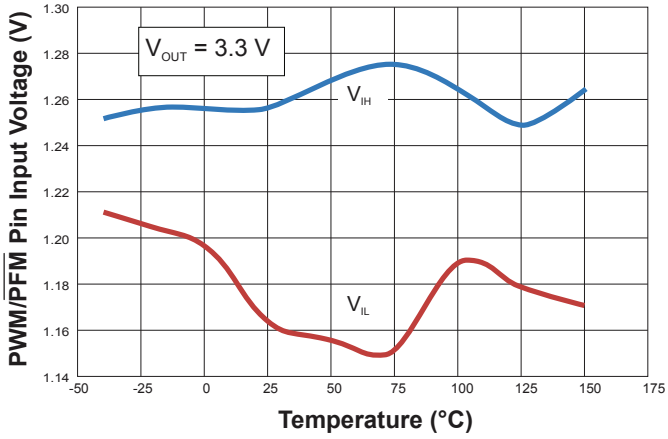
Error Amplifier Transconductance versus Temperature



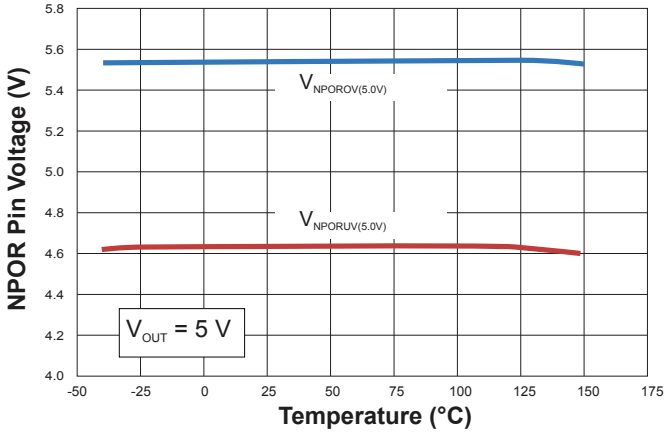
PWM/$\overline{\text{PFM}}$ High and Low Voltage Thresholds versus Temperature



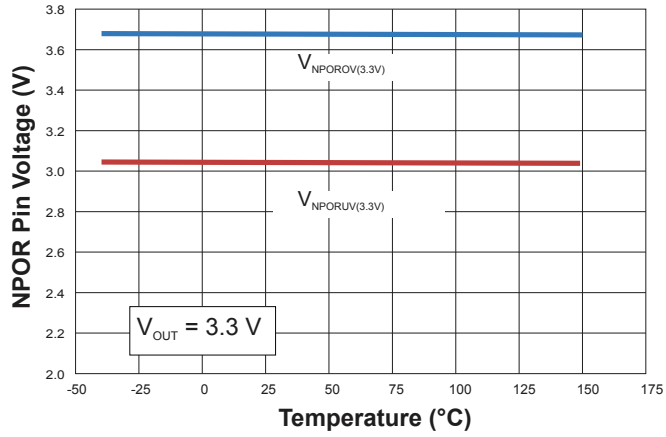
PWM/$\overline{\text{PFM}}$ High and Low Voltage Thresholds versus Temperature



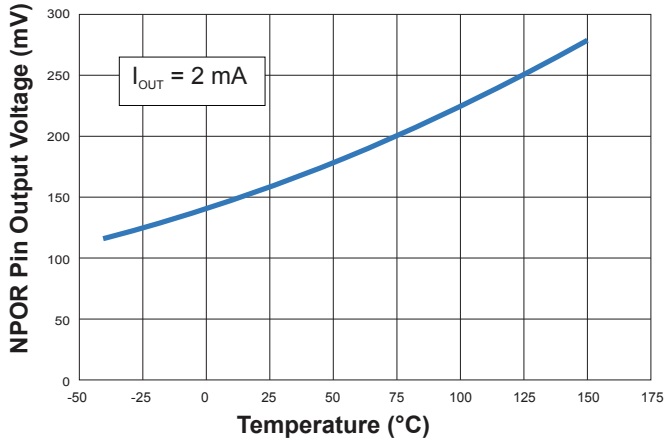
NPOR Overvoltage and Undervoltage Thresholds versus Temperature



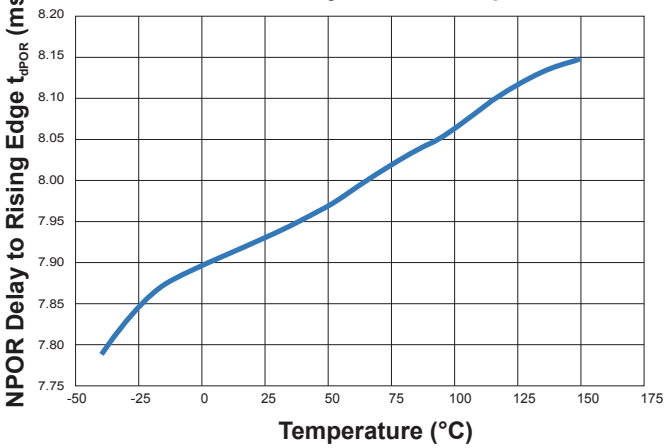
NPOR Overvoltage and Undervoltage Thresholds versus Temperature



NPOR Low Output Voltage versus Temperature

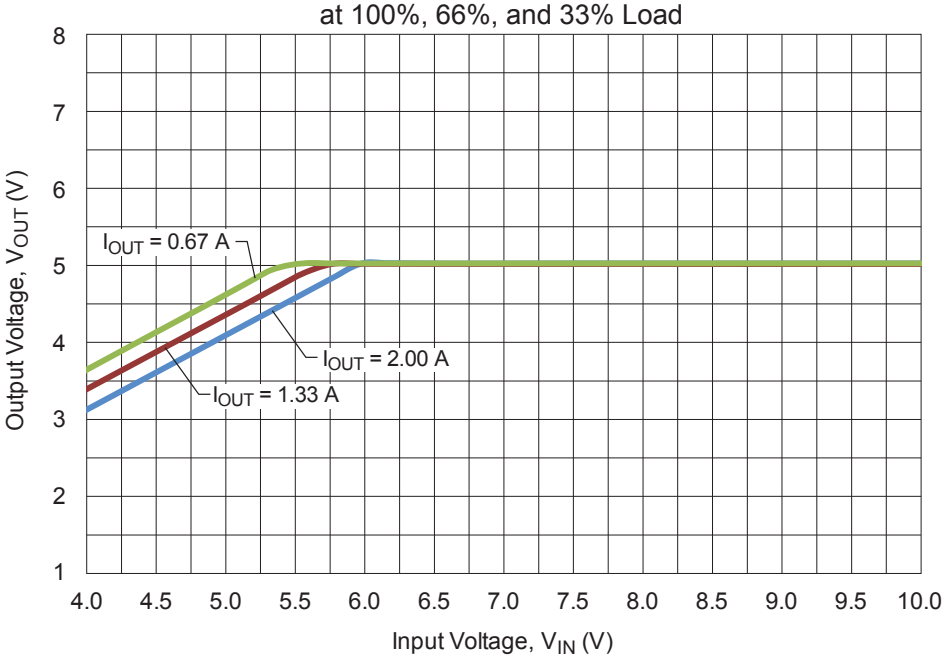


NPOR Time Delay versus Temperature

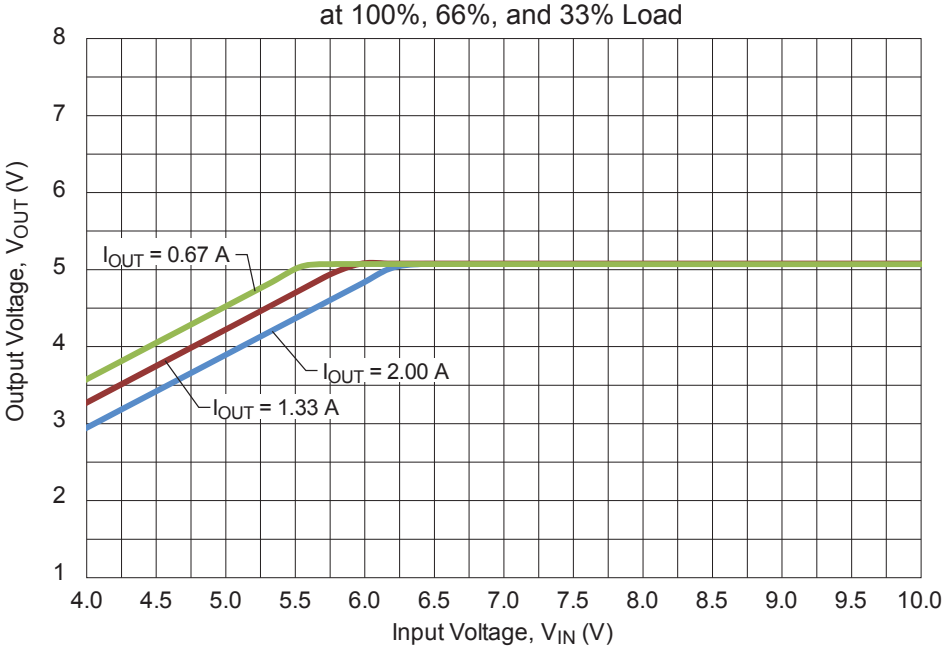


DROPOUT OPERATION – TYPICAL AND WORST CASE OPERATION

Typical Output Voltage versus Input Voltage at High Ambient at 100%, 66%, and 33% Load



Worst Case Output Voltage versus Input Voltage at High Ambient at 100%, 66%, and 33% Load



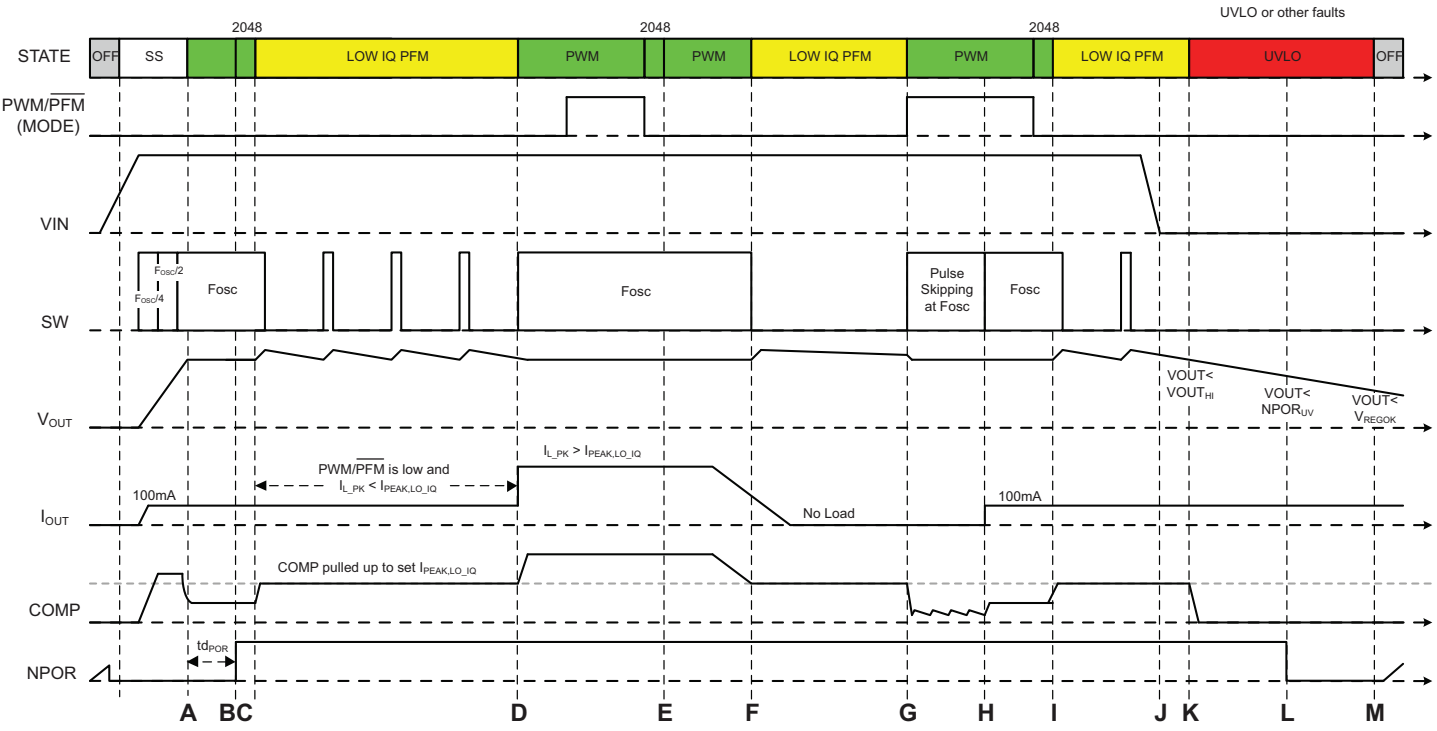


Figure 1: PWM/PFM Mode Timing Diagram

A The output voltage reaches regulation voltage after soft start startup. The A8585 family always starts in PWM mode, independent of the PWM/PFM signal.

B NPOR transitions high after NPOR delay (7.5 ms (typ)).

C PWM/PFM signal is logic low, so the device enters Low I_Q PFM mode after NPOR transitions high and 2048 clock cycles expire.

D The output current increases and, even though PWM/PFM is low, the device transitions to PWM mode to maintain optimal regulation.

E PWM/PFM transitions low after transitioning high, 2048 clock cycles occur, but the device stays in PWM mode because the output current is too high.

F The output current decreases and PWM/PFM has been low for a relatively long time, so the device enters Low I_Q PFM mode.

G PWM/PFM transitions high so the device is forced into PWM mode immediately, independent of the load current. If the output is at no load condition, then the device starts pulse skipping with COMP hovering around the 400mV pedestal.

H The output current increases from no load condition, and the device stops pulse skipping and starts switching again at f_{OSC}.

I The output current is low, PWM/PFM transitions low, and 2048 clock cycles later, the device enters Low I_Q PFM mode due to low current.

J V_{IN} has been removed but the circuit is still powered from the VOUT pin. In addition, all faults are ignored while $V_{OUT} > V_{OUTHI}$.

K When V_{OUT} drops below $VOUT_{HI}$ (1% above the regulation point) all faults are checked. UVLO is active, so the COMP pin is pulled low and switching is disabled.

L When V_{OUT} drops below the V_{NPORUV} threshold, NPOR transitions low.

M When V_{OUT} drops below V_{REGOV}, the device is completely turned off.

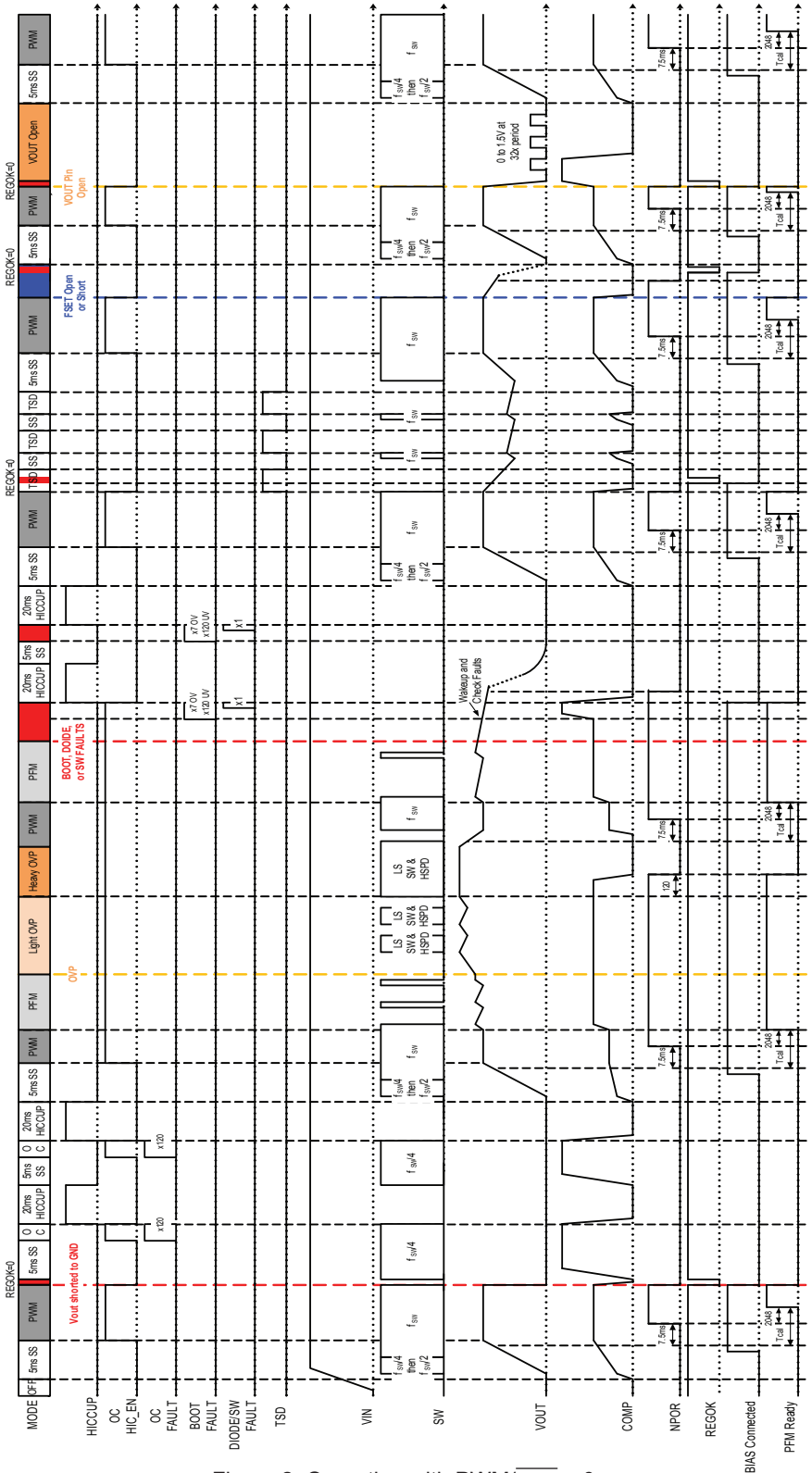


Figure 2: Operation with PWM/$\overline{\text{PFM}}$ = 0

FUNCTIONAL DESCRIPTION

Overview

The A8585 family are current mode, buck regulators that incorporate all the control and protection circuitry necessary to provide the power supply requirements of car audio and infotainment systems.

The A8585 family consists of four parts:

Part Number	PWM Mode Selection*	10 µA Sleep Mode	Output Voltage (V)
A8585	yes	no	5.0
A8585-1	yes	no	3.3
A8585-2	(automatic)	yes	5.0
A8585-3	(automatic)	yes	3.3

*A synchronization signal on the FSET pin, or a heavy output load current will force all variants into PWM mode.

The A8585 family has three modes of operation:

- Pulse width modulation (PWM) mode, delivering up to 2.0 A. (All variants)
- Low-I_Q pulse frequency modulation (PFM) mode, drawing only approximately 10 µA from V_{IN} while maintaining V_{OUT} (at no load). Under most conditions, Low-I_Q PFM mode is typically capable of supporting up to approximately 100 mA, depending on applications. (All variants)
- For the A8585-2 and A8585-3 variants, a third mode of operation is entered when the EN/$\overline{\text{SLEEP}}$ pin is set to 0. The device enters an ultra-low current, shutdown mode. V_{OUT} = 0 V and the total current drawn from V_{IN} is less than 10 µA (typ).

In PFM mode, the device operates with lower switching frequency to achieve higher efficiency at light load. When the load is heavy, the device automatically transitions into PWM mode to support a relatively higher current. For the A8585 and A8585-1 variants, setting the PWM/PFM pin high disables PFM operation mode even at light load and forces the device to operate in a PWM constant frequency mode.

The A8585 family is designed to support up to 2.0 A output. However, the exact amount of current it will supply, before possible thermal shutdown, depends heavily on duty cycle, ambient temperature, airflow, PCB layout, and PCB construction. Figure 3 shows calculated current ratings versus ambient temperature for V_{IN} = 12 V/V_{OUT} = 3.3 V and for V_{IN} = 12 V/V_{OUT} = 5.0 V at 300 kHz and 550 kHz. This analysis assumed a 4-layer PCB according to the JEDEC standard (34°C/W), no nearby heat sources, and no airflow.

Reference Voltage

The A8585 family incorporates an internal reference. The accuracy of the internal reference is ±1.0% for T_J from 0°C to 85°C, and ±1.5% from −40°C to 150°C. The output voltage from the device regulator is directly connected to the VOUT pin and is divided down internally to 800 mV by an internal resistor divider inside the regulator, as shown in the Functional Block diagram. The A8585 and A8585-2 variants have a fixed 5.0 V output voltage; the A8585-1 and A8585-3 variants have a fixed 3.3 V output voltage.

PWM Switching Frequency

The PWM switching frequency of the A8585 family is adjustable from 300 to 550 kHz and has an accuracy of ±10% over the operating temperature range. The switching frequency is dithered to help reduce EMI between -7.5% and 7.5% according to a random sequence.

During startup, the PWM switching frequency changes from 25%, to 50%, and finally 100% of f_{SW} as V_{OUT} rises from 0 V to the regulation voltage. The startup switching frequency is described in detail in the Soft Start section of this datasheet.

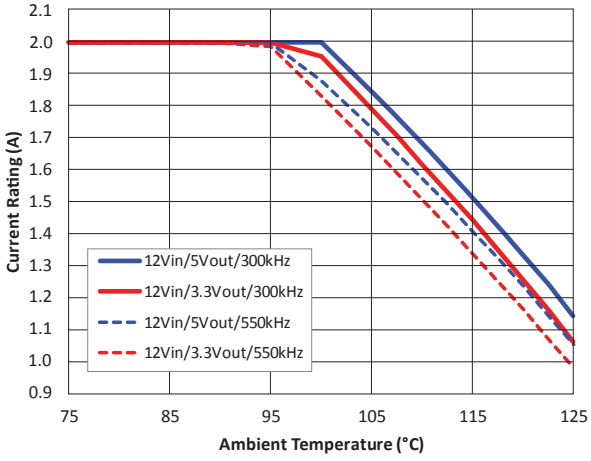


Figure 3: Typical Current Derating

If the regulator output is shorted to ground, $V_{FB} \approx 0$ V and the PWM frequency is 25% of f_{SW}. In this case, the low switching frequency allows extra off-time between SW pulses. The extra off-time allows the inductor current to remain under control (remains well above 0) before the next SW pulse occurs. This prevents the inductor current from ratcheting up, or rising, to a value that could damage the device or the output inductor.

The FSET pin includes protection features that disable the regulator when the FSET pin is shorted to GND, shorted High (to NPOR), or when RFSET is mis-selected.

EN/$\overline{\text{SLEEP}}$ Input (for A8585-2 and A8585-3)

The A8585-2 and A8585-3 variants have the EN/$\overline{\text{SLEEP}}$ logic level input pin. To enable the device, the EN/$\overline{\text{SLEEP}}$ pin must be a logic high (>2.1 V). The EN/$\overline{\text{SLEEP}}$ pin is rated to 40 V so this EN/$\overline{\text{SLEEP}}$ pin may be connected directly to V_{IN} if there is no suitable logic signal available to wake up the regulator.

When EN/$\overline{\text{SLEEP}}$ transitions low, the device waits approximately 224 µs before shutting down. This delay provides plenty of filtering to prevent the device from prematurely entering Sleep mode because of any small glitches that might couple onto the PCB trace or EN/$\overline{\text{SLEEP}}$ pin.

PWM/$\overline{\text{PFM}}$ Input (for A8585 and A8585-1)

The PWM/$\overline{\text{PFM}}$ pin provides two major functions. This pin is a control input that sets the operating mode. If PWM/$\overline{\text{PFM}}$ is logic high the device operates only in PWM mode. If PWM/$\overline{\text{PFM}}$ is logic low the device operates in Low-I_Q PFM mode if two conditions are met: (1) the regulator is lightly loaded and (2) there is no clock signal applied to the FSET/$SYNC_{PWM}$ input pin. If PWM/$\overline{\text{PFM}}$ transitions from logic high to logic low, the device checks that $V_{SS} > 2.3$ V and NPOR = 1. If these two conditions are satisfied then the device will wait 2048 clock cycles and then enter into Low I_Q PFM mode. This delay provides sufficient filtering to prevent the regulator from prematurely entering PFM mode because of any small glitches that might couple onto the PCB trace or PWM/$\overline{\text{PFM}}$ pin.

PWM Synchronization

If an external clock is applied to the FSET/$SYNC_{PWM}$ pin, the device is forced into PWM mode and synchronizes its PWM frequency to the external clock. Synchronization is independent of Rfset it only needs to satisfy the >200 KHz requirement. When synchronizing, the external clock pulses must satisfy the pulse width, duty-cycle, and rise/fall time requirements shown in the Electrical Characteristics table in this datasheet. During synchronization, frequency dithering is disabled.

The 8585 synchronizes to the SYNC input when the FSET/$SYNC_{PWM}$ pin is driven above the 1.2 V threshold. Synchronization must occur within 16 µs or else a fault may be declared causing SW to halt operation. The 8585 will transition back to using the RFSET resistor after a rising has not crossed the 1.2V threshold for ~8 µs, resulting in the high side switch remaining off for ~8 µs and causing some VOUT droop.

Transconductance Error Amplifier

The transconductance error amplifier's primary function is to control the regulator output voltage. The error amplifier is shown in the Functional Block diagram. It is shown as a three-terminal input device with two positive inputs and one negative input. An on-chip resistor divider is included. The negative input is simply connected to the internal resistor divider and is used to sense the feedback voltage for regulation. The two positive inputs are used for soft start and steady-state regulation. The error amplifier performs an analog OR selection between the two positive inputs. The error amplifier regulates to either the internal soft start voltage or the device internal reference, whichever is lower.

To stabilize the regulator, a series RC compensation network (RZ and CZ) must be connected from the error amplifier output (the COMP pin) to GND, as shown in the Typical Application diagram. In most instances an additional, relatively low value capacitor (CP) should be connected in parallel with the RZ-CZ components to reduce the loop gain at very high frequencies. However, if the CP capacitor is too large, the phase margin of the converter can be reduced. Calculating RZ, CZ, and CP is covered in detail in the Component Selection section of this datasheet.

If a fault occurs or the regulator is disabled, the COMP pin is pulled to GND via approximately 1 kΩ and SW switching is inhibited.

Slope Compensation

The A8585 family incorporates internal slope compensation (S_E) to allow PWM duty cycles above 50% for a wide range of input/output voltages and inductor values. The slope compensation signal is added to the sum of the current sense amplifier output and the PWM ramp offset. As shown in the Electrical Characteristics table, the amount of slope compensation scales with the nominal switching frequency (f_{SW}) set by R_{FSET}. The amount of slope

compensation scales with the SYNC input frequency centered around 0.35 A/µs at 425 kHz in a similar way with RFSET.

The value of the output inductor should be chosen such that S_E is between 0.5 × and 1 × the falling slope of the inductor current (S_F).

Current Sense Amplifier

The A8585 family incorporates a high-bandwidth current sense amplifier to monitor the current in the high-side MOSFET. This current signal is used by both the PWM and PFM control circuitry to regulate the MOSFET peak current. The current signal is also used by the protection circuitry to prevent damage to the device.

Power MOSFETs

The A8585 family includes a 40 V, 110 mΩ high-side N-channel MOSFET capable of delivering at least 2.0 A. The device also includes a 10 Ω, low-side MOSFET to help insure the boot capacitor is always charged. The typical $R_{DS(on)}$ increase versus temperature is shown in Figure 4.

BOOT Regulator

The A8585 family contains a regulator to charge the boot capacitor. The voltage across the BOOT capacitor typically is 5.0 V. If the boot capacitor is missing the device detects a boot overvoltage. Similarly, if the BOOT capacitor is shorted the device detects a boot undervoltage. Also, the boot regulator has a current limit to protect itself during a short circuit condition. The details of how each type of boot fault is handled by the A8585 are shown in Table 1.

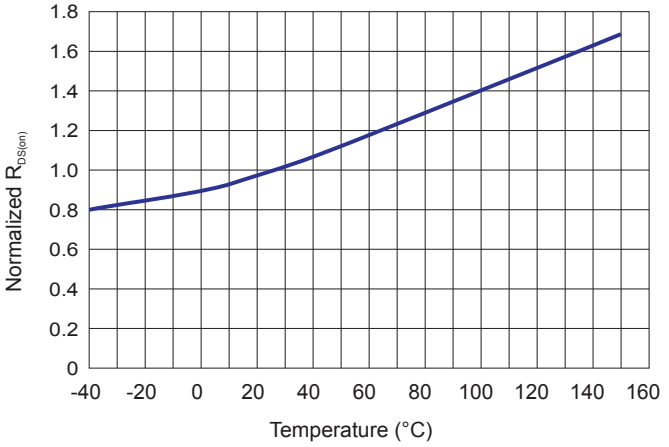


Figure 4: Typical MOSFET $R_{DS(on)}$ versus Temperature

Pulse Width Modulation (PWM) Mode

The A8585 family utilizes fixed-frequency, peak current mode control to provide excellent load and line regulation, fast transient response, and ease of compensation.

A high-speed comparator and control logic, capable of typical pulse widths down to $T_{on(min)}$, are included in the device. The inverting input of the PWM comparator is connected to the output of the error amplifier. The non-inverting input is connected to the sum of the current sense signal, the slope compensation, and a DC offset voltage ($V_{PWMOFFS}$, nominally 400 mV).

At the beginning of each PWM cycle, the CLK signal sets the PWM flip-flop and the high-side MOSFET is turned on. When the summation of the DC offset, slope compensation, and current sense signal, rises above the error amplifier voltage the PWM flip-flop is reset and the high-side MOSFET is turned off.

The PWM flip-flop is reset dominant so the error amplifier may override the CLK signal in certain situations. For example, at very light loads or extremely high input voltages the error amplifier (temporarily) reduces its output voltage below the 400 mV DC offset and the PWM flip-flop ignores one or more of the incoming CLK pulses. The high-side MOSFET does not turn on and the regulator skips pulses to maintain output voltage regulation.

In PWM mode, and when SW is switching in PFM mode, all of the device fault detection circuits are active. See Figure 1 showing how faults are handled during PWM mode. Also, the Protection Features section of this datasheet provides a detailed description of each fault and Table 1 presents a summary.

Low-I_Q Pulse Frequency Modulation (PFM) Mode

The PWM/$\overline{\text{PFM}}$ variants (A8585 and A8585-1) enter Low-I_Q PFM mode 2048 counts after the PWM/$\overline{\text{PFM}}$ pin goes low, provided that no faults are present, the load is light, NPOR = 1 and no external clock is applied to the FSET/SYNC_{PWM} pin. Similarly, the EN/$\overline{\text{SLEEP}}$ variants (A8585-2 and A8585-3) enter Low-I_Q PFM mode under the same conditions (except there is no PWM/$\overline{\text{PFM}}$ pin), and the EN/$\overline{\text{SLEEP}}$ pin is high. At light loads the PFM comparator, which is connected to the VOUT pin through the internal feedback resistor divider (which is the

internal FB point), modulates the frequency of the SW node to regulate the output voltage with very high efficiency.

The reference for the PFM comparator is calibrated approximately 1% above the PWM regulation point. When the voltage at the internal FB point rises above the PFM comparator threshold and peak inductor current falls below $I_{PEAK(LO\_IQ)}$ minus slope compensation, the device will enter PFM coast mode, tri-stating the SW node and drawing extremely low current from V_{IN}. When voltage at the FB point falls below the PFM comparator threshold the device will fully power-up after approximately a 2.5 µs delay and the high-side MOSFET is repeatedly turned on, operating at the PWM switching frequency until the voltage at the FB pin rises above the PFM comparator threshold. V_{OUT} will rise at a rate determined by, and have a voltage ripple dependent on, the input voltage, output voltage, inductor value, output capacitance, and load.

When the COMP pin falls to a voltage corresponding to the Low-I_Q Peak Current Threshold ($I_{PEAK(LO\_IQ)}$) value, an internal clamp prevents the COMP voltage from falling further. This results in the output voltage rising slightly which causes the PFM comparator to trip and the device to enter the PFM Coast mode. Thus when the load demands a peak inductor current that corresponds to less than the Low-I_Q Peak Current Threshold ($I_{PEAK(LO\_IQ)}$) minus the impact of slope compensation at the given duty cycle the device operates in PFM mode. This transition point from PWM to PFM mode is defined by the input voltage, output voltage, slope compensation, and inductor value.

Figure 5 demonstrates PFM mode operation for a light load (5 mA). Figure 6 shows PWM and Low I_Q PFM transitions. In PFM mode the load steps from 0.05A (PFM operation) to 1.05A (PWM operation) and then transitions back to 0.05A PFM mode.

Soft Start (Startup) and Inrush Current Control

Inrush current is controlled by the internal embedded soft start function. The soft start time of the A8585 family is fixed at 5 ms. When the device is enabled and all faults are cleared, the internal soft start voltage ramps upward from 0 V. When the soft start voltage exceeds the equivalent VOUT voltage the error amplifier output slews above the 400 mV pedestal initiating PWM switching.

When the device begins switching, the error amplifier regulates the internal FB voltage to be the soft start voltage. During the active portion of soft start, the regulator output voltage rises from 0 V to the nominal value.

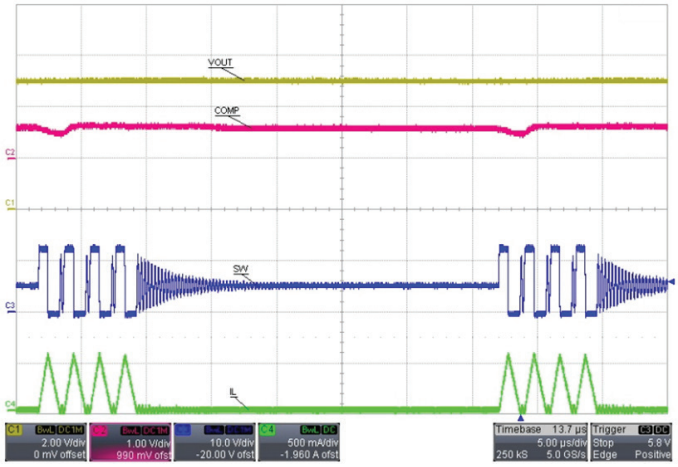


Figure 5: PFM Mode at Light Load (5 mA)
V_{IN} = 12 V, V_{OUT} = 5.0 V

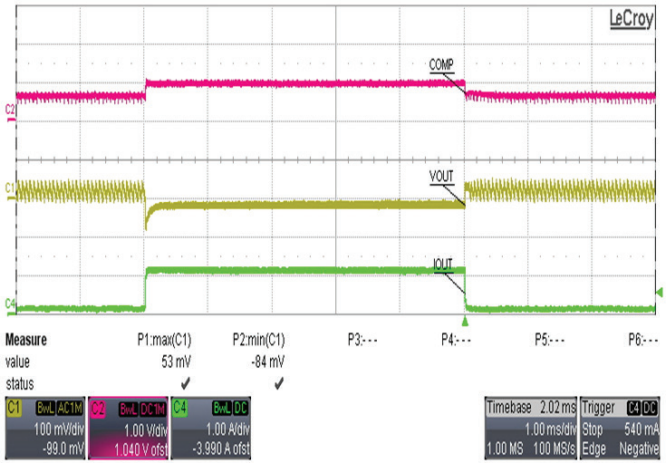


Figure 6: Load Steps Between 0.05 A and 1.05 A in PFM Mode

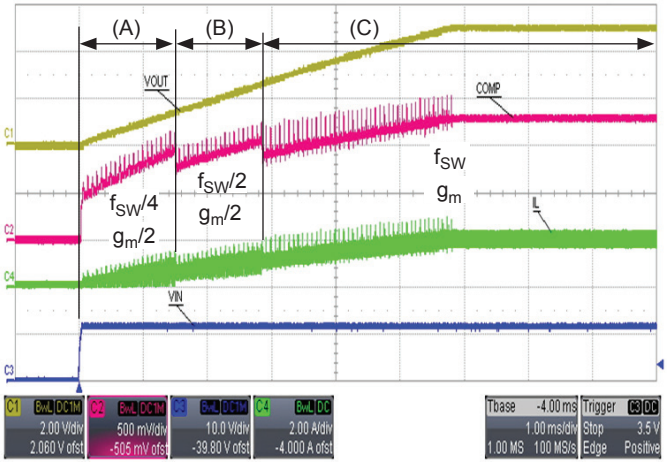


Figure 7: Soft Start Operation
V_{OUT} Ramps from Startup (VIN powered) to Nominal (5.0 V at 2.0 A, for A8585/A8585-2, shown)

In Figure 7 the startup sequence shows the soft start operation. During startup, while VOUT voltage is below 25% (interval A in Figure 7) the PWM switching frequency is reduced to 1/4 of f_{SW}. This corresponds to V_{OUT} < 1.25 V (for nominal 5.0 V output: A8585/A8585-2) or < 0.825 V (for nominal 3.3 V output: A8585-1/A8585-3). While VOUT is above 25% but below 50% (interval B) the switching frequency is reduced to 1/2 of f_{SW}, and when VOUT is above 50% (at C) the switching frequency is f_{SW}.

The error amplifier gain (g_m) also changes. While VOUT is below 50% (at A through B) g_m is reduced to $g_m/2$. While VOUT is above 50% (at C) the error amplifier gain is g_m.

The reduced switching frequencies and error amplifier gain are necessary to help improve output regulation and stability when V_{OUT} is very low. When V_{OUT} is very low the PWM control loop requires on-times near the minimum controllable on-time, and extra low duty cycles that are not possible at the nominal switching frequency. When the soft start voltage reaches approximately 800 mV, the error amplifier switches over to referencing the device internal 800 mV reference for regulating the internal (resistor divider) FB voltage.

If the device is disabled or a fault occurs, the internal fault latch is set, and the soft start voltage is discharged to ground very quickly. When the soft start voltage decays to approximately 200 mV, the device clears the internal fault latch.

The soft start voltage is discharged slowly when the device is in hiccup mode. Therefore, the soft start not only determines the startup time but also the time between soft start attempts in hiccup mode. Hiccup mode operation is discussed in more details in the Protections section of this datasheet.

Pre-Biased Startup

If the output of the regulator is pre-biased to some voltage, the A8585 family modifies the normal startup routine, in order to prevent discharging the output capacitors. As described previously, the error amplifier usually becomes active when the soft start voltage starts to ramp. If the output is pre-biased, the internal FB voltage is at some non-zero voltage. The COMP pin remains low and SW is tri-stated until the soft start voltage rises above the V_{FB}. Figure 8 shows startup when the output voltage is pre-biased to 2.0 V.

Active Low Power-On Reset (NPOR) Output

The A8585 family has an inverted Power-On Reset output (NPOR) with a fixed delay (t_{dPOR}) before the rising edge. The NPOR output is an open drain output so an external pull-up resistor must be used, as shown in the Typical Application diagram.

NPOR transitions high when the output voltage is within regulation. In PWM mode, NPOR is high when the output voltage is typically within 92.5% to 110% of the target value. The NPOR overvoltage and undervoltage comparators incorporate a small amount of hysteresis ($V_{NPORUV(HYS)(xV)}$), 40 mV(typ) for 3.3 V output variants (A8585-1/A8585-3) and 60 mV (typ) for 5.0 V output variants (A8585/A8585-2), and filtering (5 µs, typical) to help reduce chattering.

The NPOR output is immediately pulled low if either an overvoltage or an undervoltage condition occurs, or if the device junction temperature exceeds the Thermal Shutdown Threshold (T_{SDth}). For other faults, NPOR depends on the output voltage. Table 1 summarizes all of the A8585 family fault modes and the effects on NPOR. When powering down, if VIN goes low before VOUT, NPOR will pulled low when the undervoltage condition occurs, but will only remain low while VOUT remains above ~3.0V.

For the variants with selectable Sleep mode (A8585-2 and A8585-3), when the EN/$\overline{\text{SLEEP}}$ pin goes low switching stops after 224 µs (typ) (t_{dSLEEP}), and NPOR goes low (even if $V_{OUT} > V_{NPORUV}$) and stays low until V_{OUT} drops to about 25% of nominal value. When V_{OUT} falls to about 25% of its nominal value, the device goes into Sleep mode consuming $I_{IN(SLEEP)}$ on VIN, and shortly after that, NPOR will be released (no longer pulled low). Given this operation, the time that NPOR remains low is dependent on the current consumption on VOUT and the output capacitance. It is important to note that the high-side switch leakage can overwhelm the load current on VOUT, especially since the IC current on VOUT is very low in this mode. Therefore for reliable operation in this situation, the user should select an

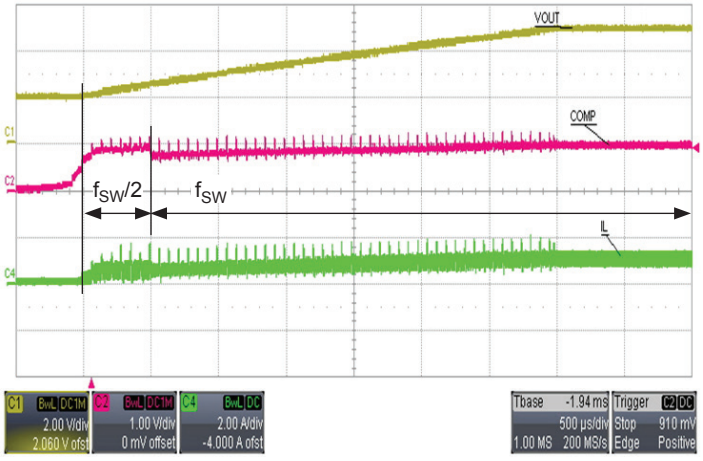


Figure 8: Soft Start Prebiased Startup
V_{OUT} Prebiased at 2 V, Ramps to Nominal (5.0 V at 2.0 A, for A8585/A8585-2, shown)

NPOR resistor (if connected to VOUT) with a low enough value to overwhelm any high-side switch leakage.

Protection Features

The A8585 was designed to satisfy the most demanding automotive and non-automotive applications. In this section, a description of each protection feature is provided, and table 1 summarizes the protection operation. All faults are available in both PWM and PFM mode. In PFM mode all faults are monitored just before and while switching is active, but are ignored while VOUT remains above the PFM comparator threshold and below the NPOR OV threshold.

UNDERVOLTAGE LOCKOUT (UVLO)

An undervoltage lockout (UVLO) comparator monitors the voltage at the VIN pin and keeps the regulator disabled if the voltage is below the stop threshold ($V_{UVLO(OFF)}$). The UVLO comparator incorporates some hysteresis ($V_{UVLO(HYS)}$) to help reduce on-off cycling of the regulator due to resistive or inductive drops in the V_{IN} path during heavy loading or during startup.

PULSE-BY-PULSE OVERCURRENT PROTECTION (OCP)

The A8585 family monitors the current of the high-side MOSFET and if the current exceeds the pulse-by-pulse overcurrent threshold (I_{LIM}) then the high-side MOSFET is turned off. Normal PWM operation resumes on the next clock pulse from the oscillator. The device includes leading edge blanking (as defined by $T_{on(min)}$ spec) to prevent false triggering of the pulse-by-pulse current limit when the high-side MOSFET is turned on initially.

Because the slope compensation ramp is added to the inductor current, the A8585 family delivers more current at lower duty cycles and less current at higher duty cycles. Figure 9 illustrates the relationship between the current limit and duty cycle. As shown, the current limit at min and max duty cycle remains fixed, but the relationship vs. duty cycle is skewed with frequency due to the fixed minoff time. Given the relationship it is best to use the $I_{LIM(tonmin)}$ and $I_{LIM(toffmin)}$ to calculate the current limit at a given duty cycle.

During synchronization, the slope compensation scales in a similar fashion as RFSET, with slight less accuracy.

The exact current the buck regulator can support is heavily dependent on duty cycle (V_{IN}, V_{OUT}, diode forward voltage V_f), ambient temperature, thermal resistance of the PCB, airflow, component selection, and nearby heat sources.

OVERCURRENT PROTECTION (OCP) AND HICCUP MODE

An OCP counter and hiccup mode circuit protect the buck regulator when the output of the regulator is shorted to ground or when the load is too high. When the soft start ramp is active (t<tss), the OCP hiccup counter is disabled. Two conditions must be met for the OCP counter to be enabled and begin counting:

- $t > t_{SS}$, and
- V_{COMP} clamped at its maximum voltage (OCL = 1)

As long as these two conditions are met the OCP counter remains enabled and counts pulses from the overcurrent comparator. If the COMP voltage decreases (OCL = 0) the OCP counter is cleared.

If the OCP counter reaches OCP_{LIM} counts (120), a hiccup latch is set and the COMP pin is quickly pulled down by a relatively low resistance (1 kΩ), and switching is halted for 20 ms to provide time for the IC to cool down. After the hiccup off-time expires (20 ms), the soft start ramp starts, marking the beginning of a new, normal soft start cycle as described earlier.

When the soft start voltage crosses the effective output voltage, the error amplifier forces the voltage at the COMP pin to quickly slew upward and PWM switching resumes. If the short circuit at the regulator output remains, another hiccup cycle occurs. Hiccups repeat until the short circuit is removed or the converter is disabled. If the short circuit has been removed, the device soft starts normally and the output voltage automatically recovers to the target level, as shown in Figure 10.

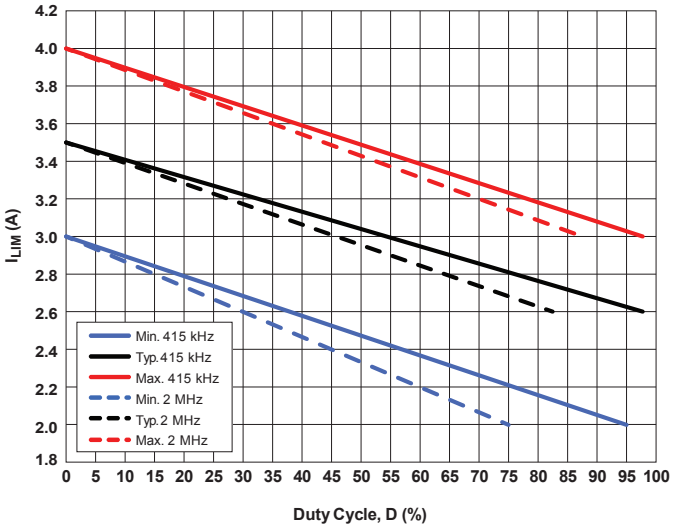


Figure 9: Pulse-by-Pulse Current Limit vs Duty Cycle at 300 kHz (dashed lines) and 550 kHz (solid lines)

BOOT CAPACITOR PROTECTION

The A8585 family monitors the voltage across the BOOT capacitor to detect if the capacitor is missing or short circuited. If the BOOT capacitor is missing, the regulator enters hiccup mode after 7 PWM cycles. If the BOOT capacitor is shorted, the regulator enters hiccup mode after 120 to 64 PWM cycles.

For a BOOT fault, hiccup mode operates virtually the same as described previously for an output short circuit fault (OCP), having a hiccup off time of 20ms followed by a soft start retry with repeated attempts until the fault clears. However, OCP is the only fault that is ignored during the soft start ramp time (t_{SS}). BOOT faults are a non-latched condition, so the device automatically recovers when the fault is corrected.

ASYNCHRONOUS DIODE PROTECTION

If the asynchronous diode is missing or damaged (open) the SW pin is subject to unusually high negative voltages. This negative voltage may cause the device to malfunction and could lead to damage. The A8585 family includes protection circuitry to detect when the asynchronous diode is missing. If the SW pin is below −1.25 V typically, for more than 50 ns typically, the device enters hiccup mode after detecting 1 missing diode fault.

Also, if the asynchronous diode is shorted, the device experiences extremely high currents through the high-side MOSFET. If this occurs, the device enters hiccup mode after detecting 1 shorted diode fault.

OVERVOLTAGE PROTECTION (OVP)

The A8585 family provides an always-on over voltage protection that monitors VOUT, to protect against VOUT rising up at light loads due to high side switch leakage. In this case, the high-side switch is forced off and the low-side switch continues to operate and can correct the OVP condition provided only a few milliamperes of pull-down current are required. When the condition causing the overvoltage is corrected, the regulator automatically recovers.

During an output overvoltage condition, the device tries for up to 120 counts (t_{dPOV_POR}) to clear the overvoltage condition. If the overvoltage condition is successfully cleared within this time period, NPOR does not go low and the device continues to operate in PFM mode. If the overvoltage fault is not cleared during this time, then an NPOR = 0 is declared and the device works indefinitely to reduce the output overvoltage fault. If it is successful in clearing this fault, then there will be an approximately 7.5 ms delay (t_{dPOR}) before NPOR pin returns high. Note that the size of the regulator output capacitor may have an effect on whether the overvoltage condition is cleared within the t_{dPOV_POR} time period.

PIN-TO-GROUND AND PIN-TO-PIN SHORT PROTECTIONS

The A8585 family is designed to satisfy the most demanding automotive applications. For example, the device is carefully designed fundamentally to withstand a short circuit to ground at each pin without suffering damage.

In addition, care was taken when defining the device pin-out to optimize protection against adjacent pin-to-pin short circuits. For example, logic pins and high voltage pins are separated as much as possible. Inevitably, some low voltage pins had to be located adjacent to high voltage pins, but in these instances the low voltage pins are designed to withstand increased voltages, with clamps and/or series input resistance, to prevent damage to the device.

THERMAL SHUTDOWN (TSD)

The A8585 family monitors internal junction temperature and stops switching and pulls NPOR low if it becomes too hot. Also, to prepare for a restart, the internal soft start voltage (V_{SS}) and the voltage at the COMP pin are pulled low until $V_{SS} < V_{SSRST}$. TSD is a non-latched fault, so the device automatically recovers if the junction temperature decreases by approximately 20°C.

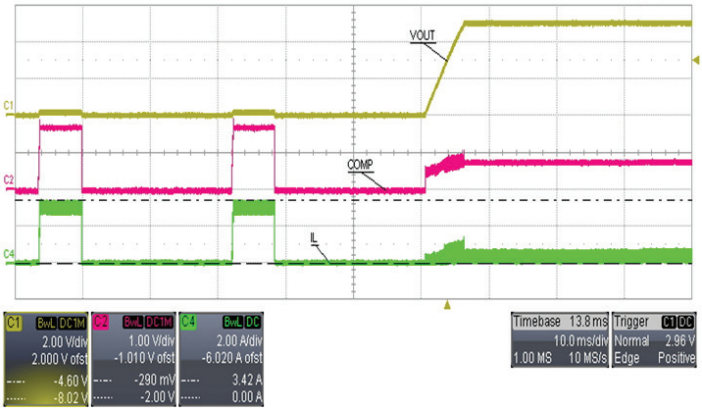


Figure 10: Hiccup Mode and Recovery
(to 5.0 V at 0.5 A, for A8585/A8585-2, shown)

Table 1: Summary of A8585 Family Fault Modes and Operation

Fault Mode	Internal Soft Start	During Fault Counting, Before Hiccup Mode			Boot Charging	NPOR	Latched Fault	Reset Condition
		V_{COMP}	High-Side Switch	Low-Side Switch				
Output shorted to ground	Hiccup, after 120 OCL faults	Clamped for I_{LIM}, then pulled low for Hiccup	$f_{OSC}/4$ due to V_{OUT} < 25%, responds to V_{COMP}	Can be activated if BOOT voltage is too low	Not affected	Depends on V_{OUT}	No	Automatic, remove the short
Output overcurrent, V_{OUT} > 50%	Hiccup, after 120 OCL faults	Clamped for I_{LIM}, then pulled low for Hiccup	f_{OSC}, responds to V_{COMP}	Can be activated if BOOT voltage is too low	Not affected	Depends on V_{OUT}	No	Automatic, decrease load current
VOUT pin open	Pulled low after 32 cycles	Pulled low after 32 cycles	Forced off by COMP low	Can be activated if BOOT voltage is to low	Not affected	Stays low	No	Automatic, V_{OUT} pin reconnected
Boot capacitor missing	Hiccup, after 7 Boot OV faults	Not affected but pulled low for Hiccup	Forced off when Boot OV fault occurs	Forced off when Boot OV fault occurs	Off after Boot fault occurs	Depends on V_{OUT}	No	Automatic, replace capacitor
Boot capacitor shorted	Hiccup, after 64 Boot UV faults	Not affected but pulled low for Hiccup	Forced off when Boot UV fault occurs	Forced off only during Hiccup	Off only during Hiccup	Depends on V_{OUT}	No	Automatic, unshort capacitor
Asynchronous diode missing	Hiccup after 1 fault	Not affected but pulled low for Hiccup	Forced off after 1 fault	Can be activated if BOOT voltage is too low	Not affected	Depends on V_{OUT}	No	Automatic, install diode
Asynchronous diode (or SW) hard short to ground	Hiccup after 1 fault	Clamped for I_{LIM}, then pulled low for Hiccup	Forced off after 1 fault	Can be activated if BOOT voltage is too low	Not affected	Depends on V_{OUT}	No	Automatic, remove short
Asynchronous diode (or SW) soft short to ground	Hiccup, after 120 OCL faults	Clamped for I_{LIM}, then pulled low for Hiccup	Active, responds to V_{COMP}	Can be activated if BOOT voltage is too low	Not affected	Depends on V_{OUT}	No	Automatic, remove short
Output overvoltage, (V_{OUT} > 3.6 V/5.5 V)	Not affected	Transitions low via loop response	Forced off	Active during $t_{OFF(MIN)}$	Off when V_{OUT} is too high	Pulled low when V_{OUT} is too high for 120 counts	No	Automatic, V_{OUT} returns to normal range
Output under voltage	Not affected	Transitions high via loop response	Active, responds to V_{COMP}	Can be activated if BOOT voltage is too low	Not affected	Pulled low when V_{OUT} is too low	No	Automatic, V_{OUT} returns to normal range
FSET shorted to GND or above 1.0 V	Pulled Low	Pulled Low	Forced Off	Forced Off	Forced Off	Depends on VOUT	No	Auto
Thermal shutdown (TSD)	Pulled low until VSS<V_{SSRST} and TSD = 0	Pulled low until VSS<V_{SSRST} and TSD = 0	Forced Off	Disabled	Off	Pulled Low	No	Auto, part cools down

Design and Component Selection

PWM Switching Frequency (R_{FSET})

The PWM switching frequency is set by connecting a resistor from the FSET/$SYNC_{PWM}$ pin to ground. Figure 11 is a graph showing the relationship between the typical switching frequency (y-axis) and the FSET resistor (x-axis). For a required switching frequency (f_{SW}), the FSET resistor value can be calculated as follows:

$$R_{FSET} = \frac{27770}{f_{SW}} - 4.78 \quad (1)$$

where f_{SW} is in kHz and R_{FSET} is in kΩ.

When the PWM switching frequency is chosen, the user should be aware of the minimum controllable on-time ($t_{ON(MIN)}$) and minimum off time of the A8585 family. If the system required on-time is less than $t_{ON(MIN)}$ then switch node jitter occurs and the output voltage has increased ripple or oscillations.

The PWM switching frequency should be calculated as follows:

$$f_{SW} = \frac{V_{OUT}}{t_{ON(MIN)} \times V_{IN(MAX)}} \quad (2)$$

where V_{OUT} is the output voltage, $t_{ON(MIN)}$ is the minimum controllable on-time of the A8585 family (100 ns (typ), 140 ns (max)), and $V_{IN(MAX)}$ is the maximum required operational input voltage (not the peak surge voltage).

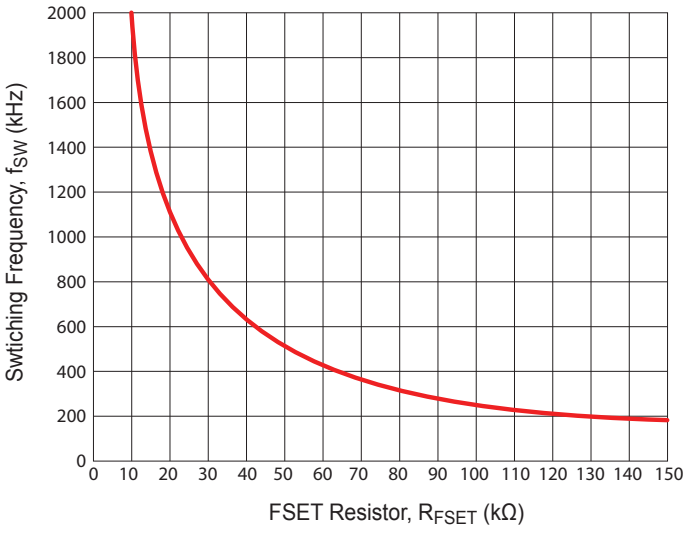


Figure 11: PWM Switching Frequency versus R_{FSET}

If the device synchronization function is employed, then the base switching frequency should be chosen such that jitter does not result at the maximum synchronized switching frequency according to equation 2.

Output Inductor (L_O)

For a peak current mode regulator it is common knowledge that, without adequate slope compensation, the system becomes unstable when the duty cycle is near or above 50%. However, the slope compensation in the A8585 family is a fixed value (S_E). Therefore, it is important to calculate an inductor value such that the falling slope of the inductor current (S_F) works well with the device slope compensation. Equations 3a and 3b can be used to calculate a range of values for the output inductor based on the well known approach of providing slope compensation that matches 50% to 100% of the down slope of the inductor current.

$$\frac{V_{OUT}+V_f}{2 \times S_E} \le L_O \le \frac{V_{OUT}+V_f}{S_E} \quad (3a)$$

where L_O is in µH, V_f is the forward voltage of the asynchronous diode, and the slope compensation (S_E) is a function of switching frequency, as follows:

$$S_E = 0.13 \times f_{SW}^2 + 0.69 \times f_{SW} + 0.031 \quad (3b)$$

where S_E is in A/µs and f_{SW} is in MHz.

More recently, Dr. Raymond Ridley presented a formula to calculate the amount of slope compensation required to critically damp the double poles at half the PWM switching frequency (this approach includes the duty cycle (D), which should be calculated at the minimum input voltage to insure optimal stability):

$$L_O \ge \frac{V_{OUT} + V_f}{S_E} \left(1 - 0.18 \times \frac{V_{IN(MIN)} + V_f}{V_{OUT} + V_f}\right) \quad (4)$$

To avoid dropout (saturation of the buck regulator), $V_{IN(MIN)}$ must be approximately 1 to 1.5 V above V_{OUT} when calculating the inductor value with equation 4.

If equations 3a or 4 yield an inductor value that is not a standard value then the next closest available value should be used. The final inductor value should allow for 10% to 20% of initial tolerance and 20% to 30% of inductor saturation.

The saturation current of the inductor should be higher than the peak current capability of the device. Ideally, for output short circuit conditions, the inductor should not saturate given the highest pulse-by-pulse current limit at minimum duty cycle ($I_{LIM(0)}$), 4.0 A (max). This may be too costly. At the very least, the inductor should not saturate given the peak operating current according to the following equation:

$$I_{PEAK} = 4.1 - \frac{S_E \times (V_{OUT} + V_f)}{1.15 \times f_{SW} \times (V_{IN(MAX)} + V_f)} \quad (5)$$

where $V_{IN(MAX)}$ is the maximum continuous input voltage, such as 18 V (not a surge voltage, like 40 V).

Starting with equation 5 and subtracting half of the inductor ripple current provides us with an interesting equation to predict the typical DC load capability of the regulator at a given duty cycle (D):

$$I_{OUT(DC)} \leq 4.1 - \frac{S_E \times D}{f_{SW}} - \frac{V_{OUT} \times (1 - D)}{2 \times f_{SW} \times L_O} \quad (6)$$

After an inductor is chosen it should be tested during output short circuit conditions. The inductor current should be monitored using a current probe. A good design should ensure the inductor or the regulator are not damaged when the output is shorted to ground at maximum input voltage and the highest expected ambient temperature.

Output Capacitors

The output capacitors filter the output voltage to provide an acceptable level of ripple voltage, and they also store energy to help maintain voltage regulation during a load transient. The voltage rating of the output capacitors must support the output voltage with sufficient design margin.

The output voltage ripple (ΔV_{OUT}) is a function of the output capacitor parameters: C_O, ESR_{CO}, and ESL_{CO}:

$$\Delta V_{OUT} = \Delta I_L \times ESR_{CO} + \frac{V_{IN} - V_{OUT}}{L_O} \times ESL_{CO} + \frac{\Delta I_L}{8 f_{SW} C_O} \quad (7)$$

The type of output capacitors determines which terms of equation 7 are dominant. For ceramic output capacitors the ESR_{CO} and ESL_{CO} are virtually zero, so the output voltage ripple will be dominated by the third term of equation 7:

$$\Delta V_{OUT} \leq \frac{\Delta I_L}{8 f_{SW} C_O} \quad (8)$$

To reduce the voltage ripple of a design using ceramic output capacitors simply: increase the total capacitance, reduce the inductor current ripple (that is, increase the inductor value), or increase the switching frequency.

For electrolytic output capacitors the value of capacitance will be relatively high, so the third term in equation 7 will be very small and the output voltage ripple will be determined primarily by the first two terms of equation 7:

$$\Delta V_{OUT} = \Delta I_L \times ESR_{CO} + \frac{V_{IN} - V_{OUT}}{L_O} \times ESL_{CO} \quad (9)$$

To reduce the voltage ripple of a design using electrolytic output capacitors simply: decrease the equivalent ESR_{CO} and ESL_{CO} by using a high(er) quality capacitor, or add more capacitors in parallel, or reduce the inductor current ripple (that is, increase the inductor value).

The ESR of some electrolytic capacitors can be quite high so Allegro recommends choosing a quality capacitor for which the ESR or the total impedance is clearly documented in the capacitor datasheet. Also, the ESR of electrolytic capacitors usually increases significantly at cold ambients, as much as 10 X, which increases the output voltage ripple and, in most cases, reduces the stability of the system.

The transient response of the regulator depends on the quantity and type of output capacitors. In general, minimizing the ESR of the output capacitance will result in a better transient response. The ESR can be minimized by simply adding more capacitors in parallel or by using higher quality capacitors. At the instant of a fast load transient (di/dt), the output voltage changes by the amount:

$$\Delta V_{OUT} = \Delta I_L \times ESR_{CO} + \frac{di}{dt} \times ESL_{CO} \quad (10)$$

After the load transient occurs, the output voltage will deviate from its nominal value for a short time. The length of this time depends on the system bandwidth, the output inductor value, and output capacitance. Eventually, the error amplifier brings the output voltage back to its nominal value.

The speed at which the error amplifier brings the output voltage back to the setpoint depends mainly on the closed-loop bandwidth of the system. A higher bandwidth usually results in a shorter time to return to the nominal voltage. However, a higher bandwidth system may be more difficult to obtain acceptable gain and phase margins. Selection of the compensation components (R_Z, C_Z, and C_P) are discussed in more detail in the Compensation Components section of this datasheet.

Low-I_Q PFM Output Voltage Ripple Calculation

After choosing an output inductor and output capacitor(s) it is important to calculate the output voltage ripple ($(\Delta V_{OUT(PFM)})$) during Low-I_Q PFM mode. With ceramic output capacitors the output voltage ripple in PWM mode is usually negligible, but that is not the case during Low-I_Q PFM mode.

The PFM mode comparator requires about 20 mV or greater of voltage ripple on the V_{OUT} pin, and generates groups of pulses to meet this requirement. However, if a single pulse results in a voltage ripple greater than 20 mV, then the voltage ripple would be dictated by that single pulse. To calculate the voltage ripple from that single pulse, first the peak inductor current must be calculated with slope compensation accounted for. The $I_{PEAK(LO\_IQ)}$ specification does not include slope compensation, therefore the peak inductor current operating point is calculated as follows:

$$I_{PEAK\_L} = \frac{I_{PEAK(LO\_IQ)}}{1 + \frac{S_E \times L_O}{V_{IN} - V_{OUT}}} \quad (11)$$

Then, calculate the MOSFET on-time and off-time (figure 12). The on-time is defined as the time it takes for the inductor current to reach I_{PEAK_L}:

$$t_{ON} = \frac{I_{PEAK\_L} \times L_O}{V_{IN} - V_{OUT} - I_{PEAK\_L} \times (R_{DS(on)HS} + L_{O(DCR)})} \quad (12)$$

where $R_{DS(on)}$ is the on-resistance of the internal high-side MOSFET (110 mΩ (typ)) and $L_{O(DCR)}$ is the DC resistance of the output inductor, L_O.

During this rising time interval, the length of time for the inductor current to rise from 0 A to I_{OUT} is:

$$t_1 = \frac{I_{OUT} \times L_O}{V_{IN} - V_{OUT} - I_{PEAK\_L} \times (R_{DS(on)HS} + L_{O(DCR)})} \quad (13)$$

The off-time is defined as the time it takes for the inductor current to decay from I_{PEAK_L} to 0 A:

$$t_{OFF} = \frac{I_{PEAK\_L} \times L_O}{V_{OUT} + V_f} \quad (14)$$

During this falling time interval, the length of time for the inductor current to fall from I_{OUT} to 0 A is:

$$t_2 = \frac{I_{OUT} \times L_O}{V_{OUT} + V_f} \quad (15)$$

Given the peak inductor current (I_{PEAK_L}) and the rise and fall

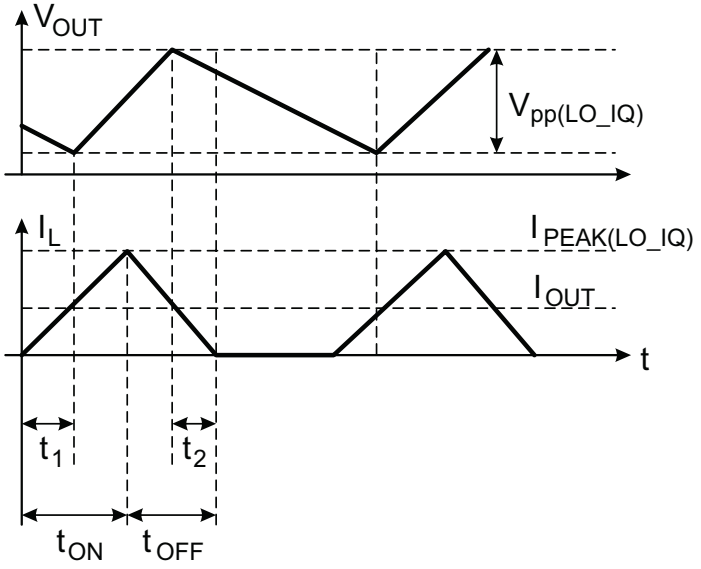


Figure 12: Illustration of Calculating the Output Ripple Voltage in PFM Mode

times (t_{ON} and t_{OFF}) for the inductor current, the output voltage ripple can be calculated for a signal pulse as follows:

$$V_{PP(LO\_IQ)} = \frac{I_{PEAK\_L} - I_{OUT}}{2 \times C_{OUT}} \times (t_{ON} + t_{OFF} - t_1 - t_2) \quad (16)$$

If $V_{PP(LO\_IQ)}$ is greater than the ~20 mV ripple that the PFM comparator requires, then the output capacitance or inductor can be adjusted to reduce the PFM mode voltage ripple. In PFM mode decreasing the inductor value reduces the PFM ripple, but may negatively impact the PWM voltage ripple, maximum load current in PWM mode, or change the mode of operation from CCM to DCM.

If $V_{PP(LO\_IQ)}$ is less than the ~20 mV requirement, the A8585 operates with multiple pulses at the PWM frequency to meet the ripple requirement. The fixed frequency operation may result in

DCM or CCM operation during the multiple pulses.

Input Capacitors

Three factors should be considered when choosing the input capacitors. First, the capacitors must be chosen to support the maximum expected input surge voltage with adequate design margin. Second, the capacitor rms current rating must be higher than the expected rms input current to the regulator. Third, the capacitors must have enough capacitance and a low enough ESR to limit the input voltage dV/dt to something much less than the hysteresis of the UVLO circuitry (nominally 400 mV for the A8585 family) at maximum loading and minimum input voltage.

The input capacitors must deliver an rms current (I_{RMS}) according to the following formula:

$$I_{RMS} = I_{OUT} \sqrt{D \times (1 - D)} \quad (17)$$

where the duty cycle (D) is defined as:

$$D \approx (V_{OUT} + V_f) / (V_{IN} + V_f) \quad (18)$$

and V_f is the forward voltage of the asynchronous diode, D1.

Figure 13 shows the normalized input capacitor rms current versus duty cycle. To use this graph, simply find the operational duty cycle (D) on the x-axis and determine the input/output current multiplier on the y-axis. For example, at a 20% duty cycle, the input/output current multiplier is 0.40. Therefore, if the regulator is delivering 2.0 A of steady-state load current, the input capacitor(s) must support 0.40 × 2.0 A or 0.8 Arms.

The input capacitor(s) must limit the voltage deviations at the VIN pin to something significantly less than the device UVLO hysteresis during maximum load and minimum input voltage. The following equation allows us to calculate the minimum input capacitance:

$$C_{IN} \geq \frac{I_{OUT} \times D \times (1 - D)}{0.85 \times f_{SW} \times \Delta V_{IN(MIN)}} \quad (19)$$

where $\Delta V_{IN(MIN)}$ is chosen to be much less than the hysteresis of the V_{IN} UVLO comparator ($\Delta V_{IN(MIN)} \leq 150$ mV is recommended), and f_{SW} is the nominal PWM frequency.

The D × (1–D) term in equation 17 has an absolute maximum

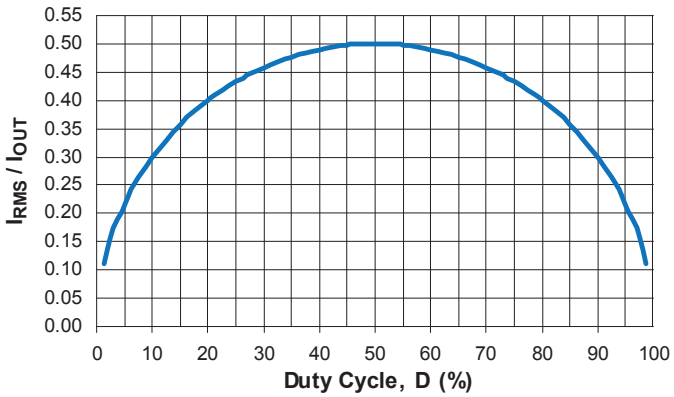


Figure 13: Normalized Input Capacitor Ripple versus Duty Cycle

value of 0.25 at 50% duty cycle. So, for example, a very conservative design based on I_{OUT} = 2.0 A, f_{SW} = 85% of 425 kHz, D × (1–D) = 0.25, and ΔV_{IN} =150 mV yields:

$$C_{IN} \geq \frac{2.0\ (A) \times 0.25}{361\ (kHz) \times 150\ (mV)} = 9.2\ \mu F$$

A good design should consider the DC-bias effect on a ceramic capacitor: as the applied voltage approaches the rated value, the capacitance value decreases. This effect is very pronounced with the Y5V and Z5U temperature characteristic devices (as much as 90% reduction), so these types should be avoided. The X5R and X7R type capacitors should be the primary choices due to their stability versus both DC bias and temperature.

For all ceramic capacitors, the DC-bias effect is even more pronounced on smaller sizes of device case, so a good design uses the largest affordable case size (such as 1206 or 1210). Also, it is advisable to select input capacitors with plenty of design margin in the voltage rating to accommodate the worst case transient input voltage (such as a load dump as high as 40 V for automotive applications).

Asynchronous Diode (D1)

There are three requirements for the asynchronous diode. First, the asynchronous diode must be able to withstand the regulator input voltage when the high-side MOSFET is on. Therefore, choose a diode with a reverse voltage rating (V_R) higher than the maximum expected input voltage (that is, the surge voltage). Second, the forward voltage of the diode (V_f) should be minimized or the regulator efficiency suffers. Also, if V_f is too high (20) the missing-diode protection in the A8585 family could be inappropriately activated. A Schottky type diode that can maintain a very low V_f when the regulator output is shorted to ground, at the coldest ambient temperature, is highly recommended. Third, the asynchronous diode must conduct the output current when the high-side MOSFET is off. Therefore, the average forward current rating of this diode ($I_{f(av)}$) must be high enough to deliver the load current according to the following equation:

$$I_{f(av)} \geq I_{OUT(MAX)} (1 - D_{MIN}) \quad (21)$$

where D_{MIN} is the minimum duty cycle, as defined in equation 19 and $I_{OUT(MAX)}$ is the maximum continuous output current of the regulator.

Bootstrap Capacitor

A bootstrap capacitor must be connected between the BOOT and SW pins to provide floating gate drive to the high-side MOSFET. Usually, 47 nF is an adequate value. This capacitor should be a high-quality ceramic capacitor, such as an X5R or X7R, with a voltage rating of at least 16 V.

The A8585 family incoporates a 10 Ω low-side MOSFET to insure that the bootstrap capacitor is always charged, even when the converter is lightly loaded or pre-biased.

Compensation Components (R_Z, C_Z, and C_P)

To properly compensate the system, it is important to understand where the buck power stage, load resistance, and output capacitance form their poles and zeros in frequency. Also, it is important to understand that the (Type II) compensated error amplifier introduces a zero and two more poles, and where these should be placed to maximize system stability, provide a high bandwidth, and optimize the transient response.

First, consider the power stage of the A8585 family, the output capacitors, and the load resistance. This circuitry is commonly referred as the *control-to-output* transfer function. The low frequency gain of this circuitry depends on the COMP to SW current gain (g_{mPOWER}), and the value of the load resistor (R_L). The DC gain ($G_{CO(0HZ)}$) of the control-to-output is:

$$G_{CO(0Hz)} = g_{mPOWER} \times R_L \quad (22)$$

The control-to-output transfer function has a pole (f_{P1}), formed by the output capacitance (C_{OUT}) and load resistance (R_L), located at:

$$f_{P1} = \frac{1}{2\pi \times R_L \times C_{OUT}} \quad (23)$$

The control-to-output transfer function also has a zero (f_{Z1}) formed by the output capacitance (C_{OUT}) and its associated ESR:

$$f_{Z1} = \frac{1}{2\pi \times ESR \times C_{OUT}} \quad (24)$$

For a design with very low-ESR type output capacitors (such as ceramic or OSCON output capacitors), the ESR zero, f_{Z1}, is usually at a very high frequency so it can be ignored. On the other hand, if the ESR zero falls below or near the 0 dB crossover frequency of the system (as happens with electrolytic output capacitors), then it should be cancelled by the pole formed by the C_P capacitor and the R_Z resistor (discussed and identified later as f_{P3}).

A Bode plot of the control-to-output transfer function for the configuration shown in the Typical Application diagram, with V_{OUT} = 5.0 V, I_{OUT} = 2.0 A, and R_L = 2.5 Ω, is shown in figure 14. The pole at f_{P1} can easily be seen at 1.2 kHz while the ESR zero, f_{Z1}, occurs at a very high frequency, 600 kHz (this is typical for a design using ceramic output capacitors). Note, there is more than 90° of total phase shift because of the double-pole at half the switching frequency.

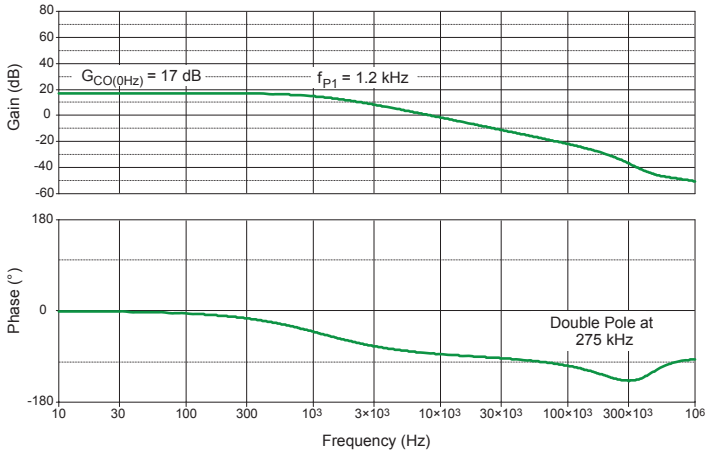


Figure 14: Control-to-Output Bode Plot

Next, consider the error amplifier (g_m), and the compensation network R_Z-C_Z-C_P. It greatly simplifies the transfer function derivation if $R_O >> R_Z$, and $C_Z >> C_P$. In most cases, $R_O > 2$ MΩ, 1 kΩ < R_Z < 100 kΩ, 220 pF < C_Z < 47 nF, and C_P < 50 pF, so the following equations are very accurate.

The low frequency gain of the control section ($G_{C(0Hz)}$) is calculated as:

$$G_{C(0\,Hz)} = g_m \times R_0 = A_{VOL} \tag{25}$$

where

V_{OUT} is the output voltage,

V_{FB} is the reference voltage (0.8 V),

g_m is the error amplifier transconductance (750 µA/V), and

R_O is the error amplifier output impedance (A_{VOL}/g_m).

The transfer function of the Type-II compensated error amplifier has a (very) low frequency pole (f_{P2}) dominated by the output error amplifier output impedance (R_O) and the C_Z compensation capacitor:

$$f_{P2} = \frac{1}{2\pi \times R_O \times C_Z} \tag{26}$$

The transfer function of the Type-II compensated error amplifier also has frequency zero (f_{Z2}) dominated by the R_Z resistor and the C_Z capacitor:

$$f_{Z2} = \frac{1}{2\pi \times R_Z \times C_Z} \tag{27}$$

Lastly, the transfer function of the Type-II compensated error amplifier has a (very) high frequency pole (f_{P3}) dominated by the R_Z resistor and the C_P capacitor:

$$f_{P3} = \frac{1}{2\pi \times R_Z \times C_P} \tag{28}$$

A Bode plot of the error amplifier and its compensation network is shown in figure 15, where f_{P2}, f_{P3}, and f_{Z2} are indicated on the Gain plot. Notice that the zero (f_{Z2} at 2.6 kHz) has been placed so that it is just above the pole at f_{P1} previously shown at 1.2 kHz in the control-to-output Bode plot (Figure 14). Placing f_{Z2} just above f_{P1} results in excellent phase margin, but relatively slow transient recovery time, as we will see later.

Finally, consider the combined Bode plot of both the control-to-output and the compensated error amplifier (Figure 16). Careful examination of this plot shows that the magnitude and phase of the entire system (red curve) are simply the sum of the error amplifier response (blue curve) and the control to output response (green curve). As shown in figure 16, the bandwidth of this system (f_c) is 60 kHz, the phase margin is 69 degrees, and the gain margin is 14 dB.

Complete designs for several common output voltages at 550 kHz, 425 kHz and 300 kHz are provided in table 2.

A Generalized Tuning Procedure

This section presents a methodology to systematically apply design considerations provided above.

1. Choose the system bandwidth (f_C). This is the frequency at which the magnitude of the gain crosses 0 dB. Recommended values for f_C, based on the PWM switching frequency, are in the range $f_{SW}/20 < f_C < f_{SW}/7.5$. A higher value of f_C generally provides a better transient response, while a lower value of f_C generally makes it easier to obtain higher gain and phase margins.

2. Calculate the R_Z resistor value. This sets the system bandwidth (f_C):

$$R_Z = f_c \times \frac{2\pi \times C_{OUT}}{g_{mPOWER} \times g_m} \tag{29}$$

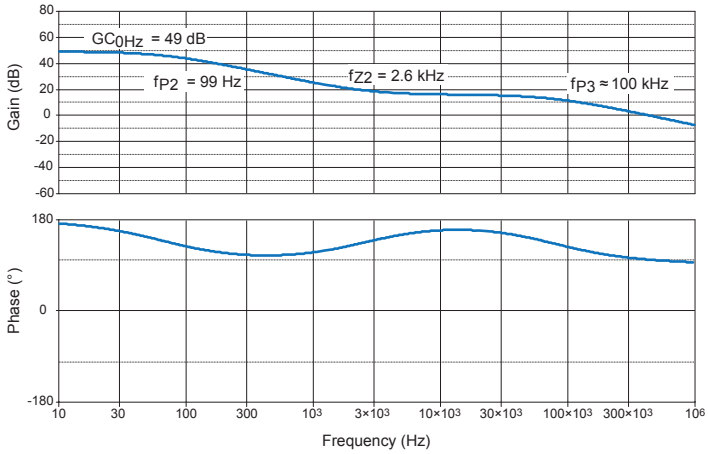


Figure 15: Type-II Compensated Error Amplifier Bode Plot

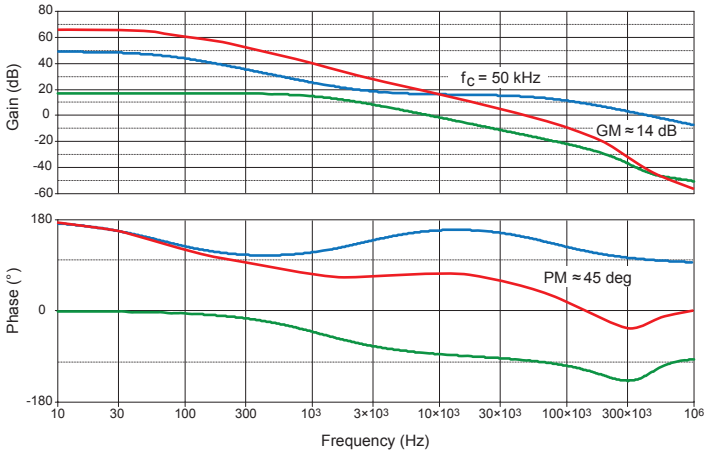


Figure 16: Bode Plot of the Complete System (red curve)

Table 2: Recommended Component Values

V_{OUT} (V)	f_{SW} (kHz)	R_{FSET} (kΩ)	L_O (µH)	C_O* (µF)	$R_Z + C_Z // C_P$			Modes
					R_Z (kΩ)	C_Z (pF)	C_P (pF)	
3.3 (A8585-1, -3)	425	59.0	10 (DR-1050-100-R)	38	34.0	560	15	PWM and PFM
5.0 (A8585, -2)			10 (DR-1050-100-R)	53	47.5	680	8	PWM and PFM
3.3 (A8585-1, -3)	550	45.3	8.2 (7447713082)	38	21.5	560	18	PWM and PFM
5.0 (A8585, -2)			10 (DR-1050-100-R)	53	60.4	1000	8	PWM and PFM
3.3 (A8585-1, -3)	300	86.6	10 (DR-1050-100-R)	38	24.9	1500	22	PWM and PFM
5.0 (A8585, -2)			22 (744770122)	53	35.7	1500	15	PWM and PFM

*The user must consider negative tolerance and DC-bias effect when choosing components to obtain C_O.

3. Determine the frequency of the pole (f_{P1}). This pole is formed by C_{OUT} and R_L. Use equation 23 (repeated here):

$$f_{P1} = \frac{1}{2\pi \times R_L \times C_{OUT}}$$

4. Calculate a range of values for the C_Z capacitor. Use the following:

$$\frac{4}{2\pi \times R_Z \times f_C} < C_Z < \frac{1}{2\pi \times R_Z \times 1.5 \times f_{P1}} \quad (30)$$

To maximize system stability (that is, to have the greatest gain margin), use a higher value of C_Z. To optimize transient recovery time, although at the expense of some phase margin, use a lower value of C_Z.

5. Calculate the frequency of the ESR zero (f_{Z1}) formed by the output capacitor(s) by using equation 24 (repeated here):

$$f_{Z1} = \frac{1}{2\pi \times \text{ESR} \times C_{OUT}}$$

If f_{Z1} is at least 1 decade higher than the target crossover frequency (f_C) then f_{Z1} can be ignored. This is usually the case for a design using ceramic output capacitors. Use equation 28 to calculate the value of C_P by setting f_{P3} to either $5 \times f_C$ or $f_{SW}/2$, whichever is higher.

Alternatively, if f_{Z1} is near or below the target crossover frequency (f_C), then use equation 28 to calculate the value of C_P by setting f_{P3} equal to f_{Z1}. This is usually the case for a design using high ESR electrolytic output capacitors.

POWER DISSIPATION AND THERMAL CALCULATIONS

The power dissipated in the A8585 family is the sum of the power dissipated from the VIN supply current (P_{IN}), the power dissipated due to the switching of the high-side power MOSFET (P_{SW}), the power dissipated due to the rms current being conducted by the high-side MOSFET (P_{COND}), and the power dissipated by the gate drivers (P_{DRIVER}).

The power dissipated from the VIN supply current can be calculated using the following equation:

$$P_{IN} = V_{IN} \times I_Q + (V_{IN} - V_{GS}) \times Q_G \times f_{SW} \quad (31)$$

where

V_{IN} is the input voltage,
I_Q is the input quiescent current drawn by the device (nominally 2.5 mA),
V_{GS} is the MOSFET gate drive voltage (typically 5 V),
Q_G is the MOSFET gate charge (approximately 2.5 nC), and
f_{SW} is the PWM switching frequency.

The power dissipated by the internal high-side MOSFET during PWM switching can be calculated using the following equation:

$$P_{SW} = \frac{V_{IN} \times I_{OUT} \times (t_r + t_f) \times f_{SW}}{2} \quad (32)$$

where

V_{IN} is the input voltage,
I_{OUT} is the output current,
f_{SW} is the PWM switching frequency, and
t_r and t_f are the rise and fall times measured at the SW node.

The exact rise and fall times at the SW node depend on the external components and PCB layout so each design should be measured at full load. Approximate values for both t_r and t_f range from 10 to 15 ns.

The power dissipated by the high-side MOSFET while it is conducting can be calculated using the following equation:

$$P_{COND} = I^2_{rms(FET)} \times R_{DS(on)HS} = \left(\frac{V_{OUT}+V_f}{V_{IN}+V_f}\right) \times \left(I^2_{OUT} + \frac{\Delta I^2_L}{12}\right) \times R_{DS(on)HS} \quad (33)$$

where

I_{OUT} is the regulator output current,
ΔI_L is the peak-to-peak inductor ripple current, and
$R_{DS(on)HS}$ is the on-resistance of the high-side MOSFET.

The $R_{DS(on)}$ of the MOSFET has some initial tolerance plus an increase from self-heating and elevated ambient temperatures. A conservative design should accommodate an $R_{DS(on)}$ with at least a 15% initial tolerance plus 0.39%/°C increase due to temperature.

The power dissipated by the internal gate drivers can be calculated using the following equation:

$$P_{DRIVER} = Q_G \times V_{GS} \times f_{SW} \quad (34)$$

where

Q_G is the gate charge to drive the MOSFET to V_{GS} = 5 V (about 2.5 nC),
V_{GS} is the gate drive voltage (typically 5 V), and
f_{SW} is the PWM switching frequency.

Bias power dissipation at VOUT pin:

$$P_{bias} = VOUT * I_{IN} = 5\ V\ (or\ 3.3\ V) * 2.5\ mA$$

Finally, the total power dissipated by the device (P_{TOTAL}) is the sum of the previous equations:

$$P_{TOTAL} = P_{IN} + P_{SW} + P_{COND} + P_{DRIVER} + P_{bias} \quad (35)$$

The average junction temperature can be calculated with the following equation:

$$T_J = P_{TOTAL} + R_{\theta JA} + T_A \quad (36)$$

where

P_{TOTAL} is the total power dissipated as described in equation 35,
$R_{\theta JA}$ is the junction-to-ambient thermal resistance (34°C/W on a 4-layer PCB), and
T_A is the ambient temperature.

The maximum junction temperature is dependent on how efficiently heat can be transferred from the PCB to ambient air. It is critical that the thermal pad on the bottom of the IC should be connected to a at least one ground plane using multiple vias.

As with any regulator, there are limits to the amount of heat that can be dissipated before risking thermal shutdown. There are trade-offs among: ambient operating temperature, input voltage, output voltage, output current, switching frequency, PCB thermal resistance, airflow, and other nearby heat sources. Even a small amount of airflow will reduce the junction temperature considerably.

PCB COMPONENT PLACEMENT AND ROUTING

A good PCB layout is critical if the A8585 family is to provide clean, stable output voltages. Follow these guidelines to insure a good PCB layout. Figure 17 shows a typical buck converter schematic with the critical power paths/loops. Figure 18 shows an example PCB component placement and routing with the same critical power paths/loops from the schematic.

1. By far, the highest di/dt in the asynchronous buck regulator occurs at the instant the high-side MOSFET turns on and the capacitance of the asynchronous Schottky diode (200 to 1000 pF) is quickly charged to V_{IN}. The ceramic input capacitors must deliver this fast, short pulse of current. Therefore the loop, from the ceramic input capacitors through the high-side MOSFET and into the asynchronous diode to ground, must be minimized. Ideally these components are all connected using only the top metal (that is, do not use vias to other power/signal layers).

2. When the high-side MOSFET is on, current flows from the input supply and capacitors, through the high-side MOSFET, into the load via the output inductor, and back to ground. This loop should be minimized and have relatively wide traces.

3. When the high-side MOSFET is off, free-wheeling current flows from ground, through the asynchronous diode, into the load via the output inductor, and back to ground. This loop should be minimized and have relatively wide traces.

4. The voltage on the SW node transitions from 0 V to V_{IN} very quickly and is the root cause of many noise issues. It is best to place the asynchronous diode and output inductor close to the device to minimize the size of the SW polygon. Also, keep low level analog signals (like FB and COMP) away from the SW polygon.

5. To have the highest output voltage accuracy, the output voltage sense trace should be connected as close as possible to the load.

6. Place the compensation components (R_Z, C_Z, and CP) as close as possible to the COMP pin. Place vias to the GND plane as close as possible to these components.

7. Place the boot strap capacitor (C_{BOOT}) near the BOOT pin and keep the routing from this capacitor to the SW polygon as short as possible.

8. When connecting the input and output ceramic capacitors, use multiple vias to GND and place the vias as close as possible to the pads of the components.

9. To minimize PCB losses and improve system efficiency, the input and output traces should be as wide as possible and be duplicated on multiple layers, if possible.

10. To improve thermal performance, place multiple vias to the GND plane around the anode of the asynchronous diode.

11. The thermal pad under the device must connect to the GND plane using multiple vias. More vias will ensure the lowest junction temperature and highest efficiency.

12. EMI/EMC issues are always a concern. Allegro recommends having component locations for an RC snubber from SW to ground. The resistor should be 1206 size.

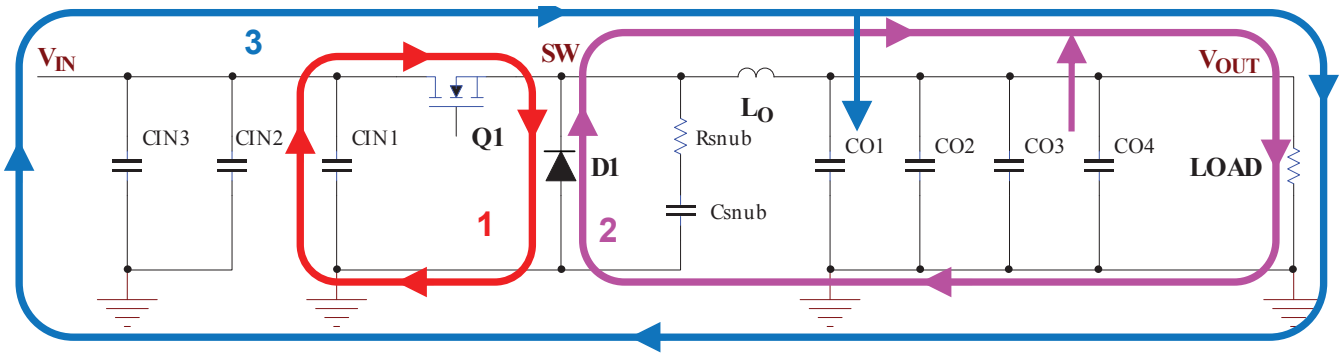


Figure 17: Typical Buck Converter with Critical Paths/Loops Shown

Loop 1 (red): At the instant Q1 turns on, Schottky diode D1, which is very capacitive, must be very quickly shut off (only 5 to 15 ns of charging time). This spike of charging current must come from the local input ceramic capacitor, CIN1. This spike of current is quite large and can be an EMI/EMC issue if the loop is not minimized. Therefore, the input capacitor CIN1 and Schottky diode D1 must be placed be on the same (top) layer, be located near each other, and be grounded at virtually the same point on the PCB.

Loop 2 (magenta): When Q1 is off, free-wheeling inductor current must flow from ground through diode D1 (SW will be at $-V_f$), into the output inductor, out to the load and return via ground. While Q1 is off the voltage on the output capacitors will decrease. The output capacitors and Schottky diode D1 should be placed on the same (top) layer, be located near each other, and be sharing a good, low inductance ground connection.

Loop 3 (blue): When Q1 is on, current flows from the input supply and input capacitors through the output inductor and into the load and the output capacitors. At this time the voltage on the output capacitors increases.

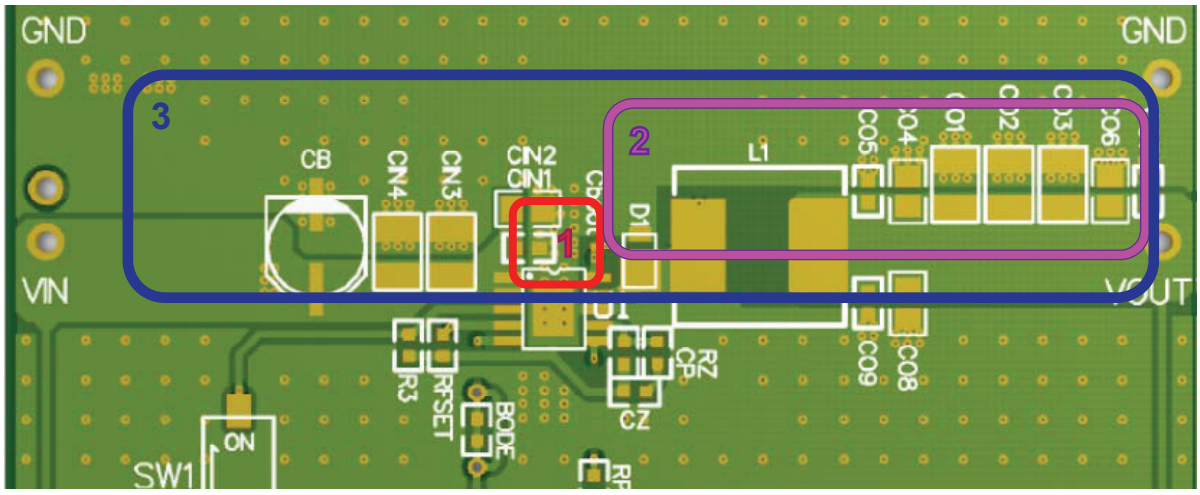


Figure 18: Example PCB Component Placement and Routing

PACKAGE OUTLINE DRAWING

For Reference Only – Not for Tooling Use

NOT TO SCALE
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

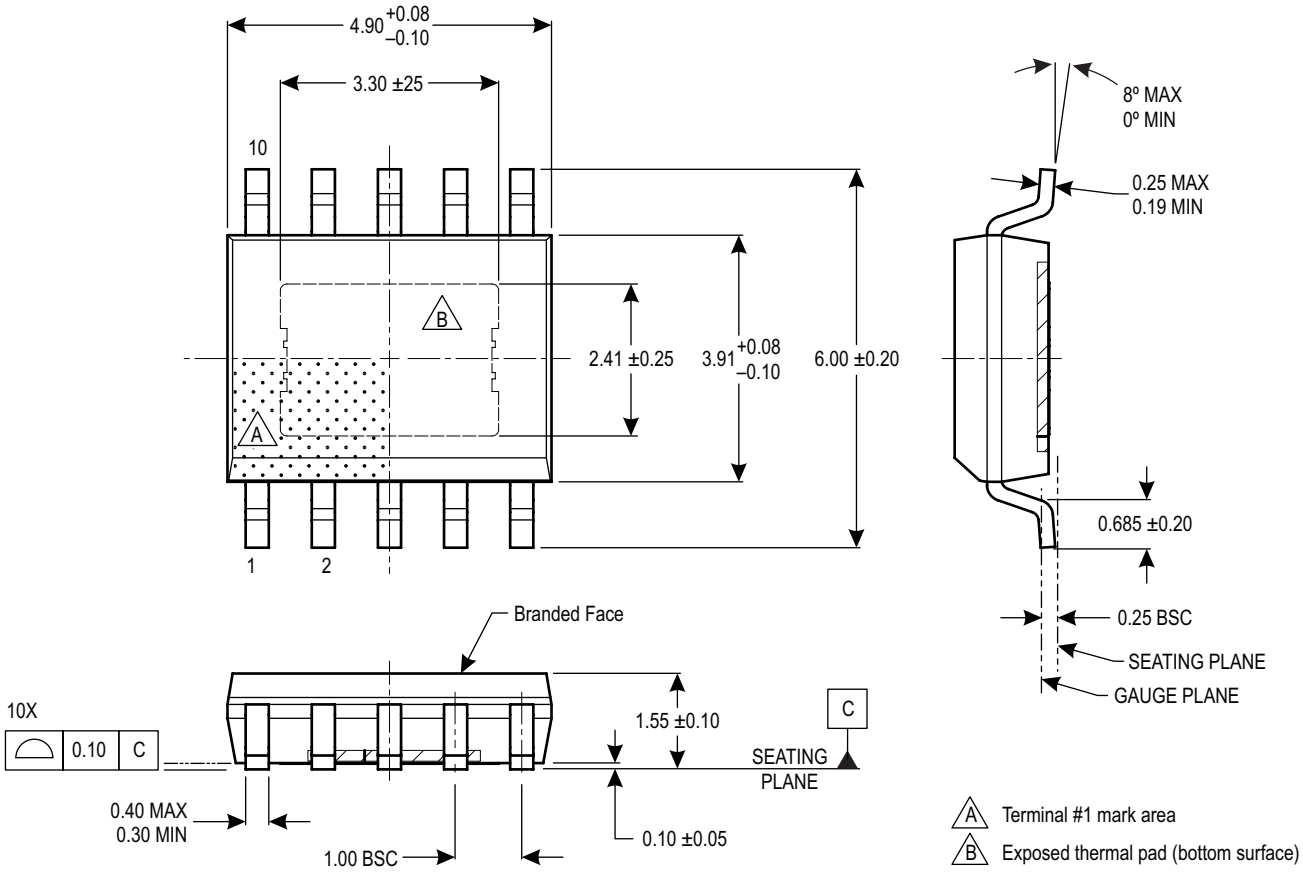


Figure 19: Package LK, 10-Pin SOIC with Exposed Thermal Pad

Revision History

Revision	Current Revision Date	Description of Revision
–	March 7, 2014	Initial Release
1	April 14, 2015	Ammended Slope Compensation values and updated Package Outline Drawing
2	May 19, 2015	Increased EN/$\overline{\text{SLEEP}}$ Delay Max value and corrected typo
3	January 8, 2016	Corrected Selection Guide part numbers